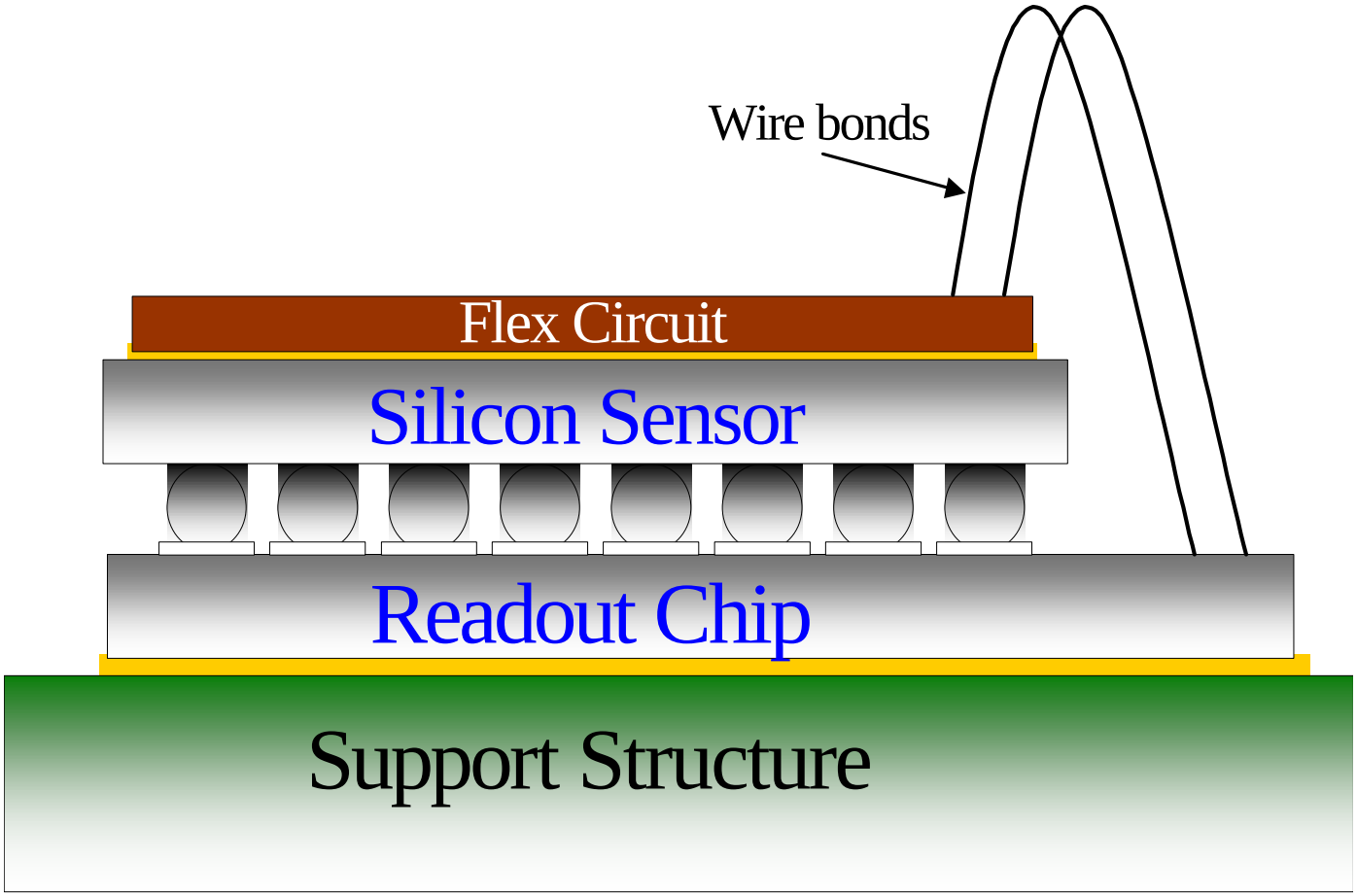
Pixel Multichip Module Prototype

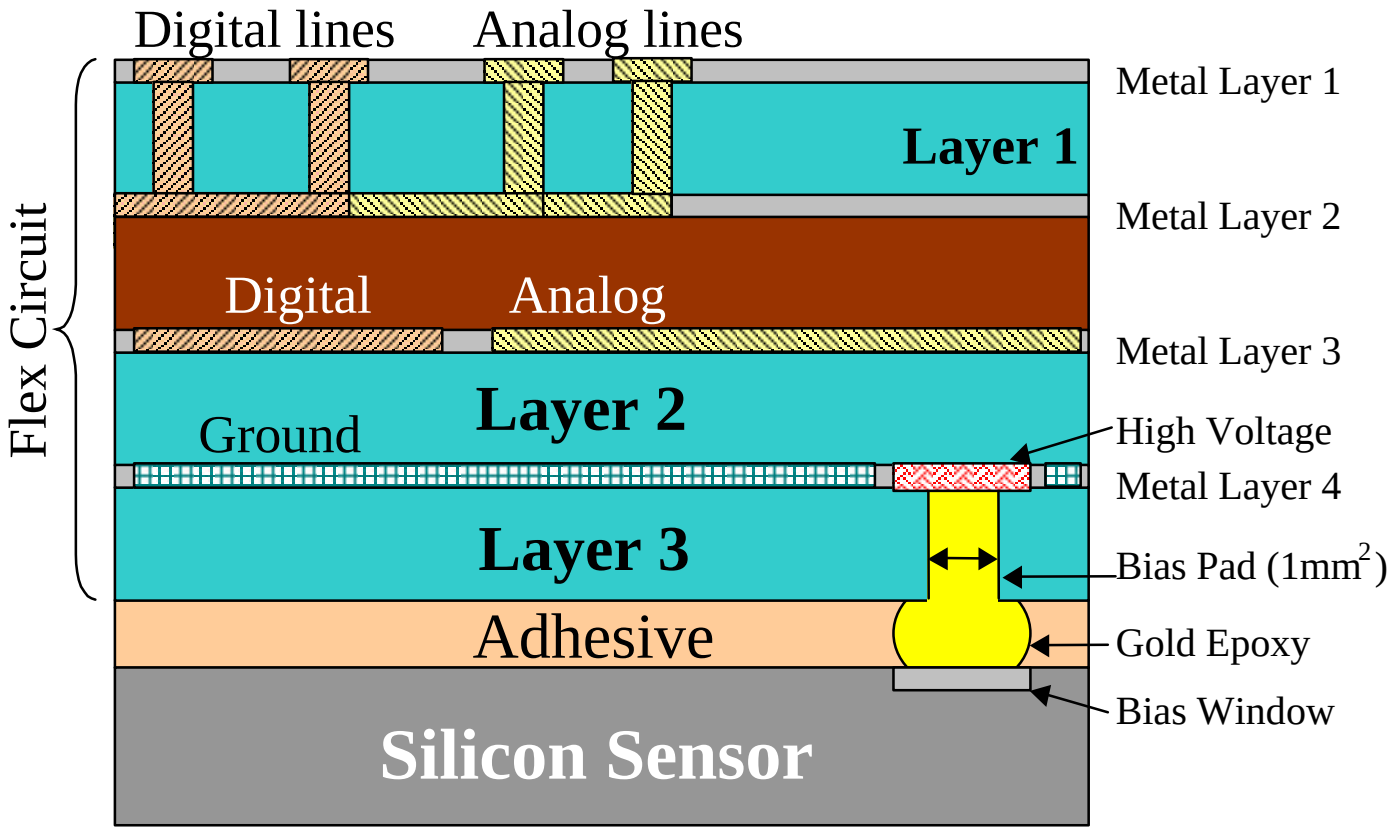
Outline

- Pixel Module Baseline
- CERN Flex Circuit
- Pixel Multichip Module Assembly
- PCI Test Stand
- Pixel Multichip Module Results
- Conclusion

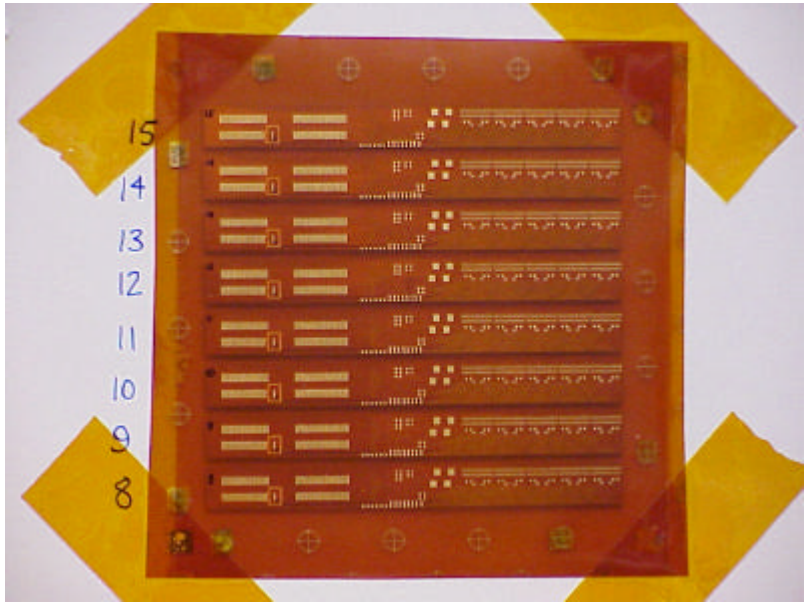
Pixel Multichip Module – Baseline Design



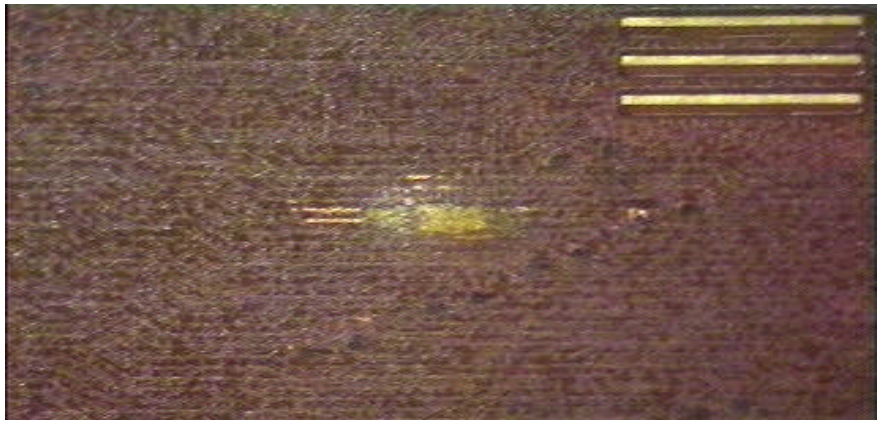
4 Layer Flex Circuit Cross Section



CERN HDI



Short Circuits



Open Vias

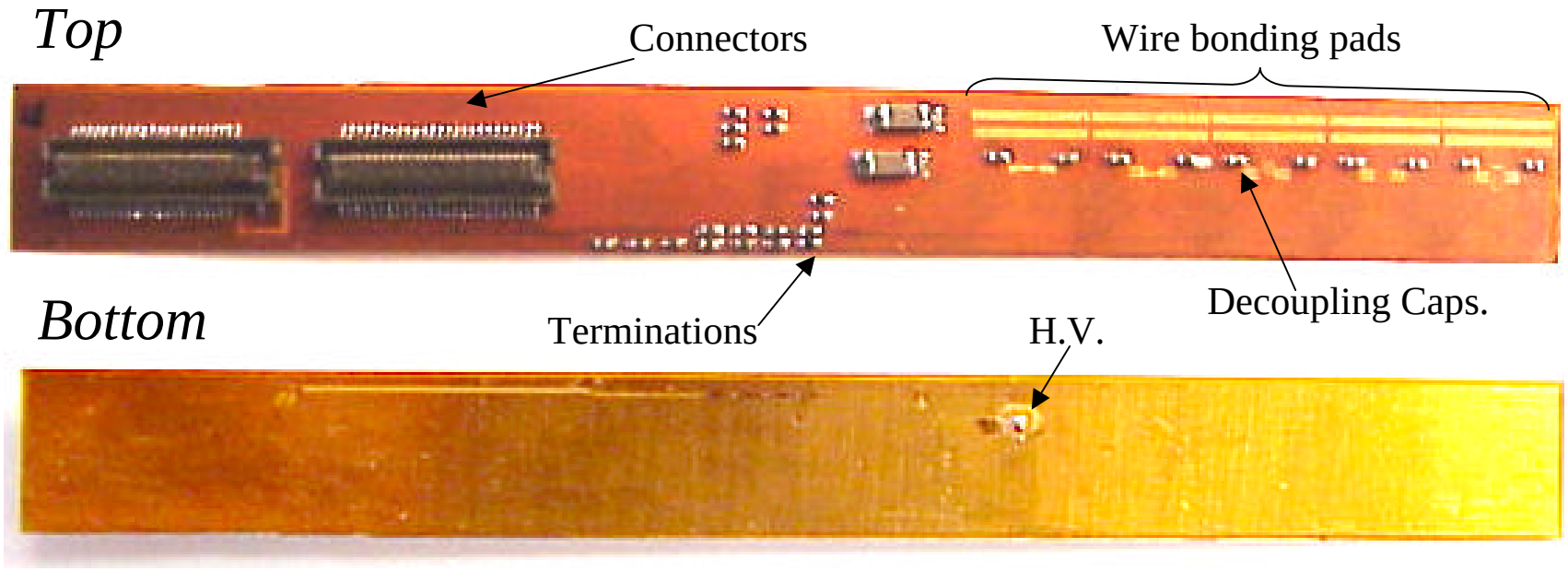
New X-ray machine @ FCC

Pixel Multichip Module Prototype

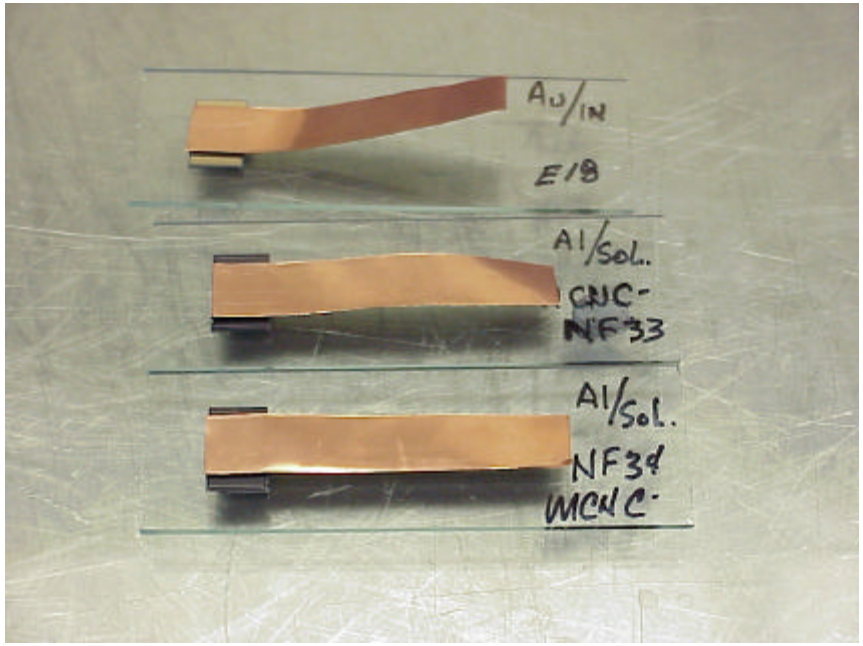
- Uses FPIX1
- Two modules characterized:
  - Single chip bump bonded to single SINTEF sensor (Indium)
  - Single chip without sensor
- Flex circuit laminated onto sensor
- Up to 5 Readout chips wire-bonded to flex circuit
- Closer to final module

Flex Circuit made by CERN

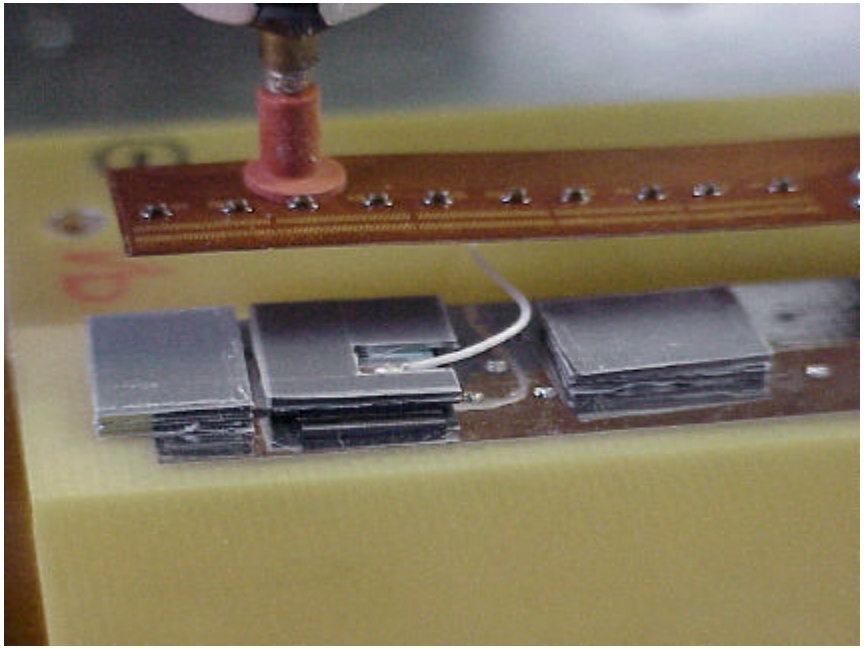
- **Dimensions:** 98.5mm x 10.25mm
- **Line width:** 35µm
- **Line to line clearance:** 35µm
- **Metal layer thickness:** 10µm
- **Number of layers:** 4
- **Via pad:** 108µm
- **Lamination:** 5µm epoxy
- **Film thickness (Apical):** 25µm

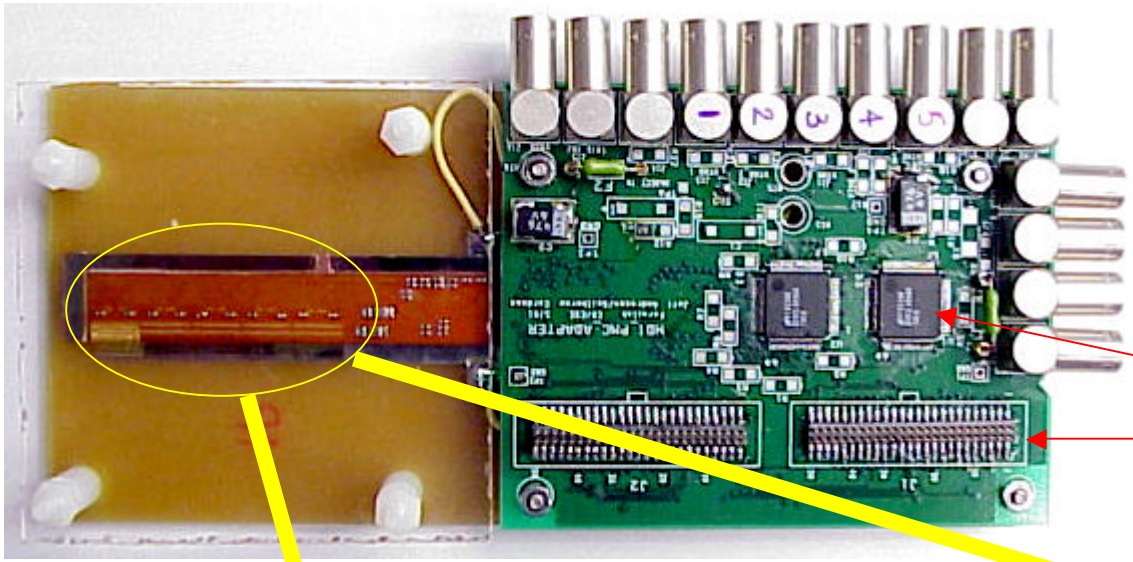


Dummy Assembly



Single Chip Assembly

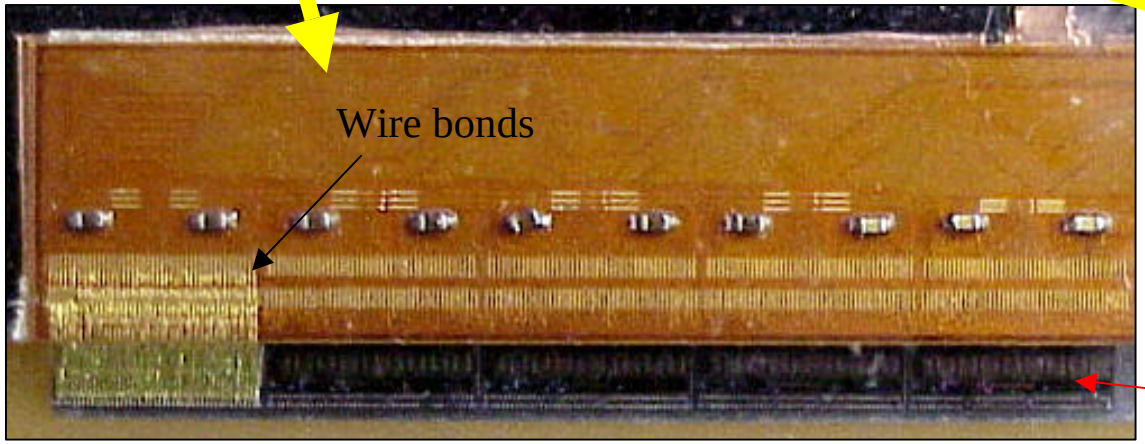


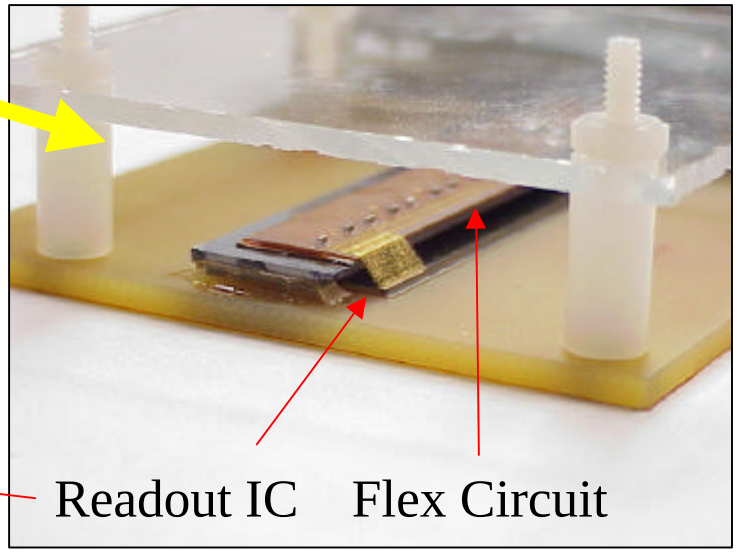


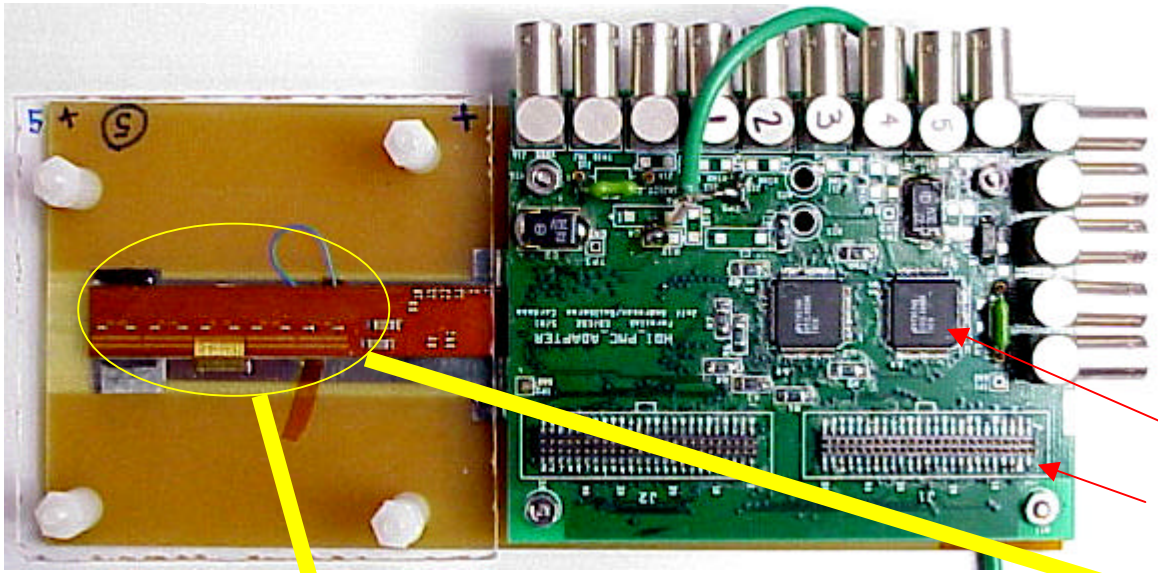
Single chip (FPIX1) without sensor

LVDS drivers

Connectors to DAQ



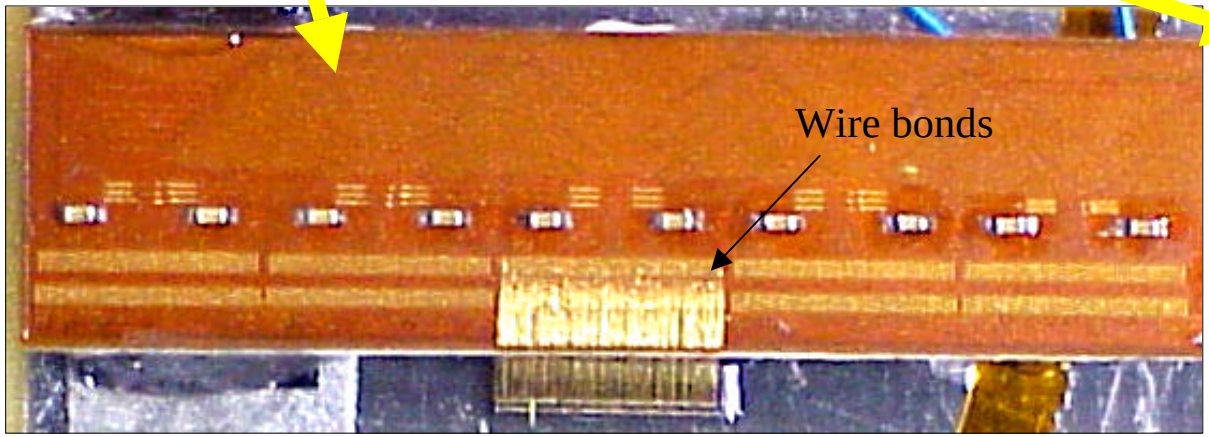


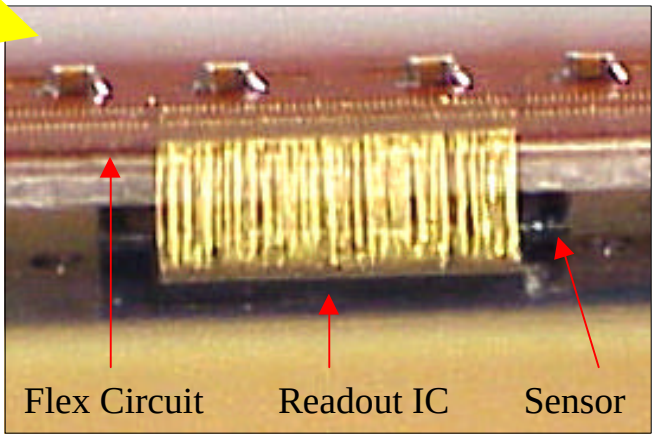


Single chip (FPIX1) with SINTEF sensor (Indium bumps)

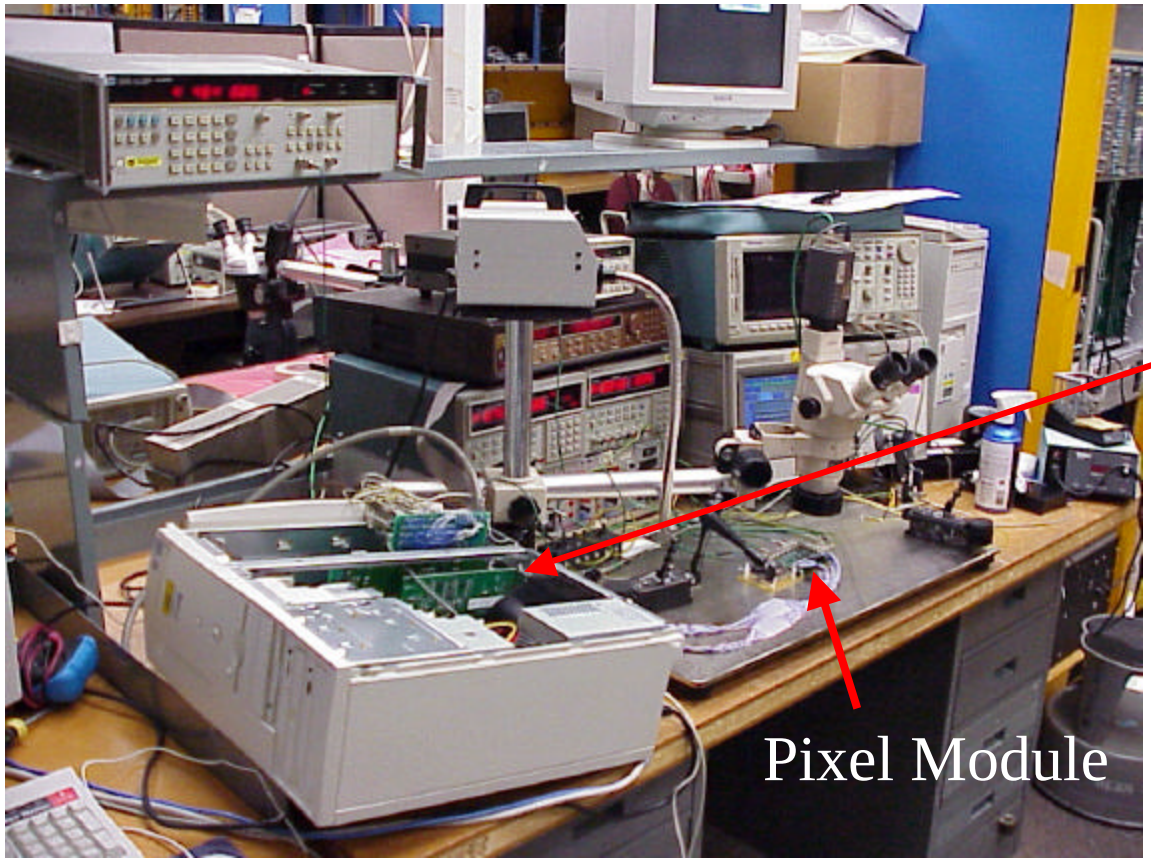
LVDS drivers

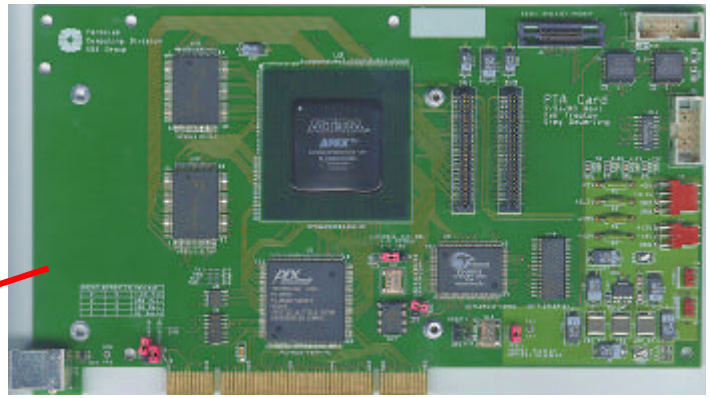
Connectors to DAQ





PCI Test Stand



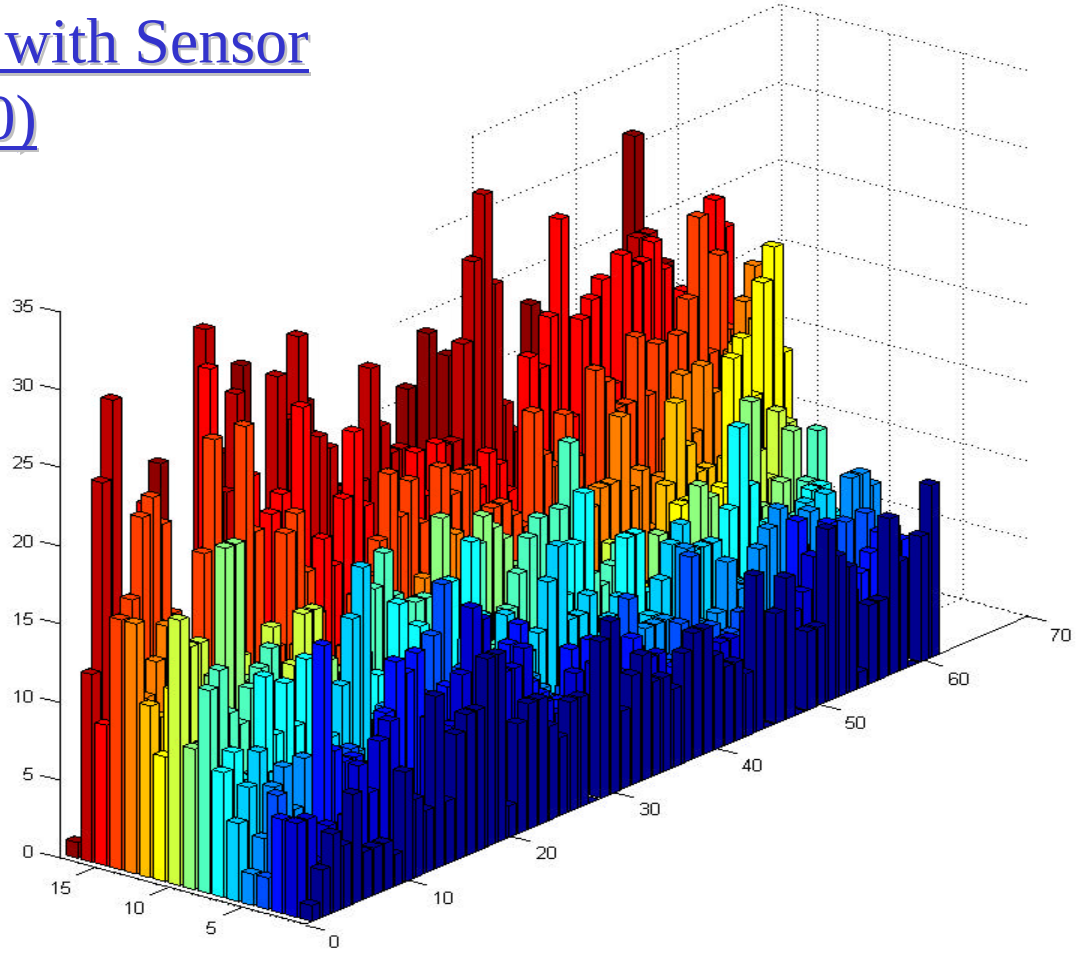


- FPGA controlling all functions
- PCI interface
- 4MB of RAM
- Daughter card interface (IEEE1386)
- JTAG
- USB
- RS232

Characterization Results [e^-]

Single Chip Without Sensor				***Single Chip With Sensor***			
μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}	μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}
7400	360	75	7	7800	410	94	7.5
6400	330	78	12	6500	390	110	11
5400	390	79	11	5500	380	110	13
4400	380	78	11	4400	380	110	15
3500	380	79	12	3300	390	120	20
2500	370	77	13	2300	390	120	21

Pixel Module with Sensor Hit Map (Sr90)



Conclusions:

- Good agreement between circuit simulation and real measurements
- Good performance characteristics.
- No significant increase in noise and threshold dispersion when compared with previous single chip prototypes
- No crosstalk problems between the digital and analog sections of the readout chip and flex circuit.