

# Irradiation tests at IUUCF in August 2001

Talk given by Gabriele Chiodini

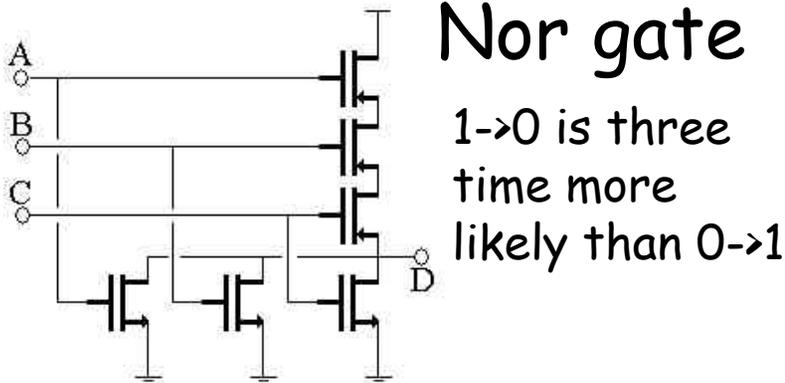
Fermilab August 20, 2001 - Monday pixel meeting

# Summary

- SEU and registers in preFPIX2Tb
- Experimental Setup
- Tests
- Results
- Estimated error in BTeV
- Conclusions
- Next

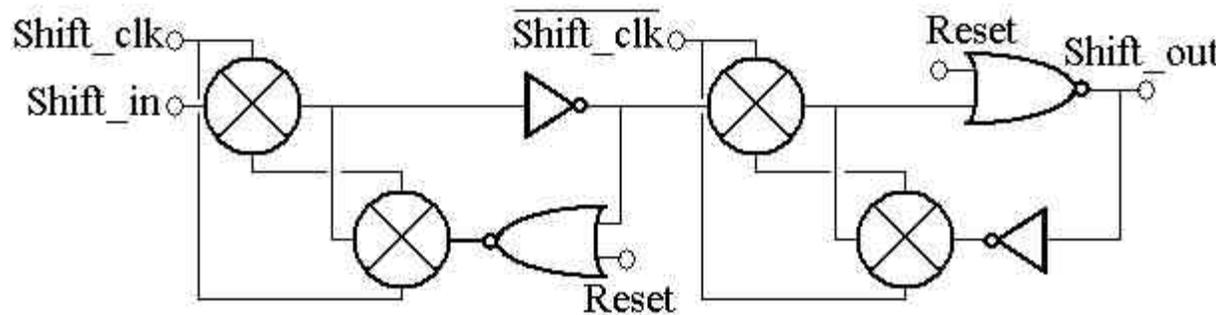
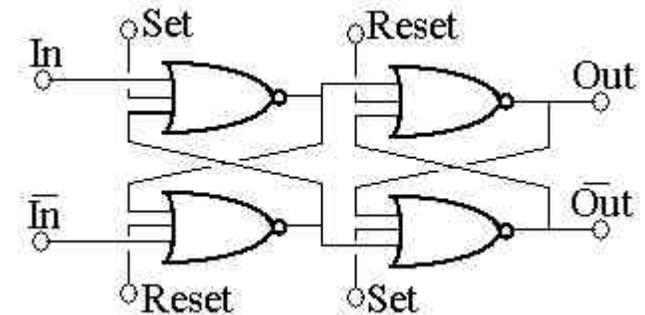
# SEU and registers in preFPIX2Tb

The Master-Slave FF's  
are build by Nor gate block:



## FF in DAC

Due to the symmetric  
configuration:  
0->1 is likely as 1->0



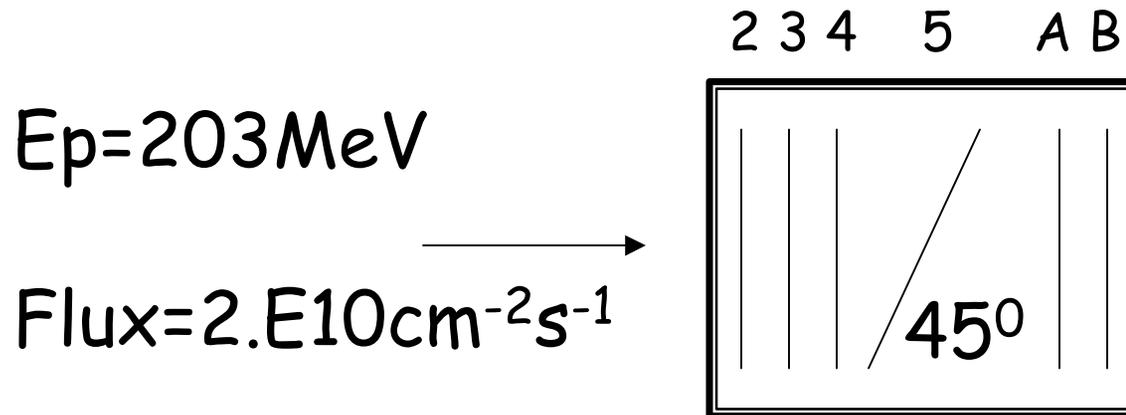
## FF in SR

Due to asymmetric  
configuration:  
1->0 is two time more  
likely than 0->1

# Experimental setup

2,3,4,5 = 4 Boards of preFPIX2Tb chip

A,B = 2 boards of 4 BTeV Sintef Sensors

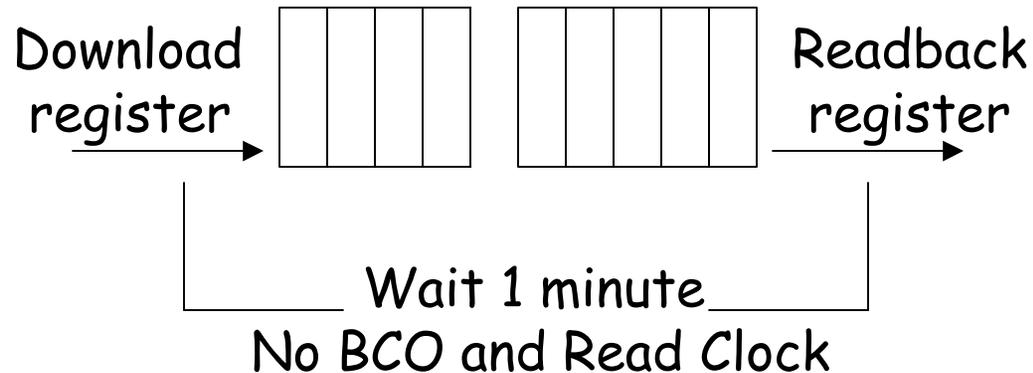


Board	2	3	4	5	A	B
TotDose [ $1\text{E}14\text{cm}^2$ ]	4.9	4.9	2.4+ 4.9	4.9	0.9	4.1
[1Mrad]	28	28	14+28=42	28	5.2	24

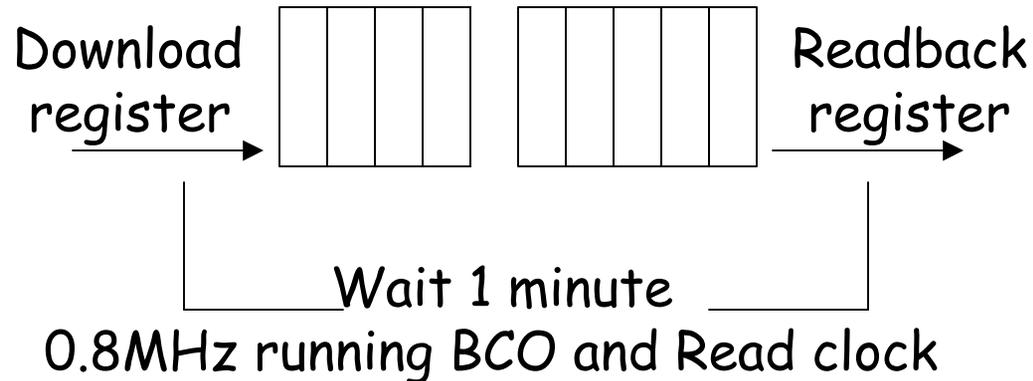
$$1\text{Mrad}(\text{Si}) = 0.58\text{E}13\text{cm}^{-2}\text{s}^{-1}$$

# Tests (a)

Test 1:

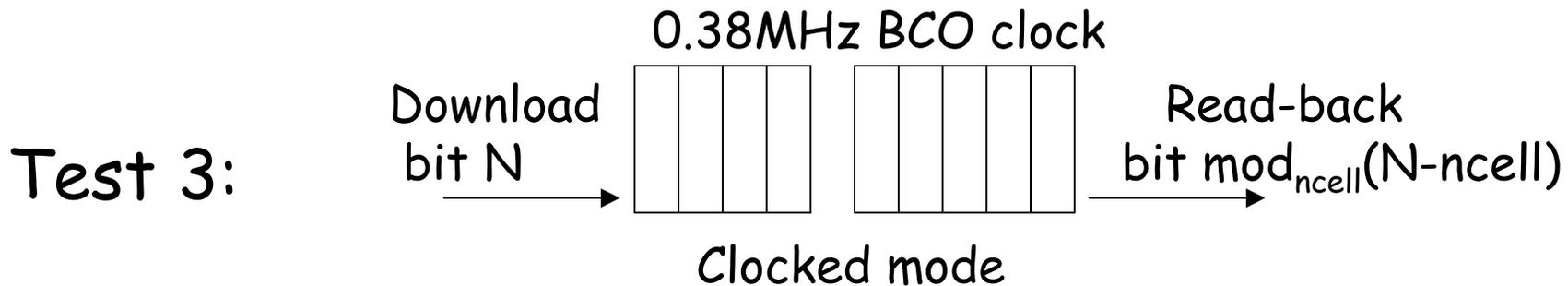


Test 2:



Most of the data have been taken with test1 and test2.  
No statistical significant difference in the results between the two tests.

# Tests (b)



- In clocked mode a SEU occurring in the Master block (first Nor gate) also contributes to the corruption of one bit. Than a factor of two in the cross section is expected in clocked-mode (Jim).
- From the electrical point of view a continuously clocked FF can have a smaller critical charge for upset increasing the SEU sensitivity of several time (Abder).

Test 3 was done for one hour out of 8 hours.

# Tests (c)

Test 4 (no reset signals must be used in this test):

1. Download the chip: no cell killed, all cell injected
2. Readout the chip.
3. Inject pulse.
4. Readout the chip.
5. Wait one minute and repeat.

Test 4 failed because when the beam was on a lot of fake hits were produced, sometime much faster that the setup could readout.

# Results: error table

Board 1 is the same as board 4 but used for irradiation test in April

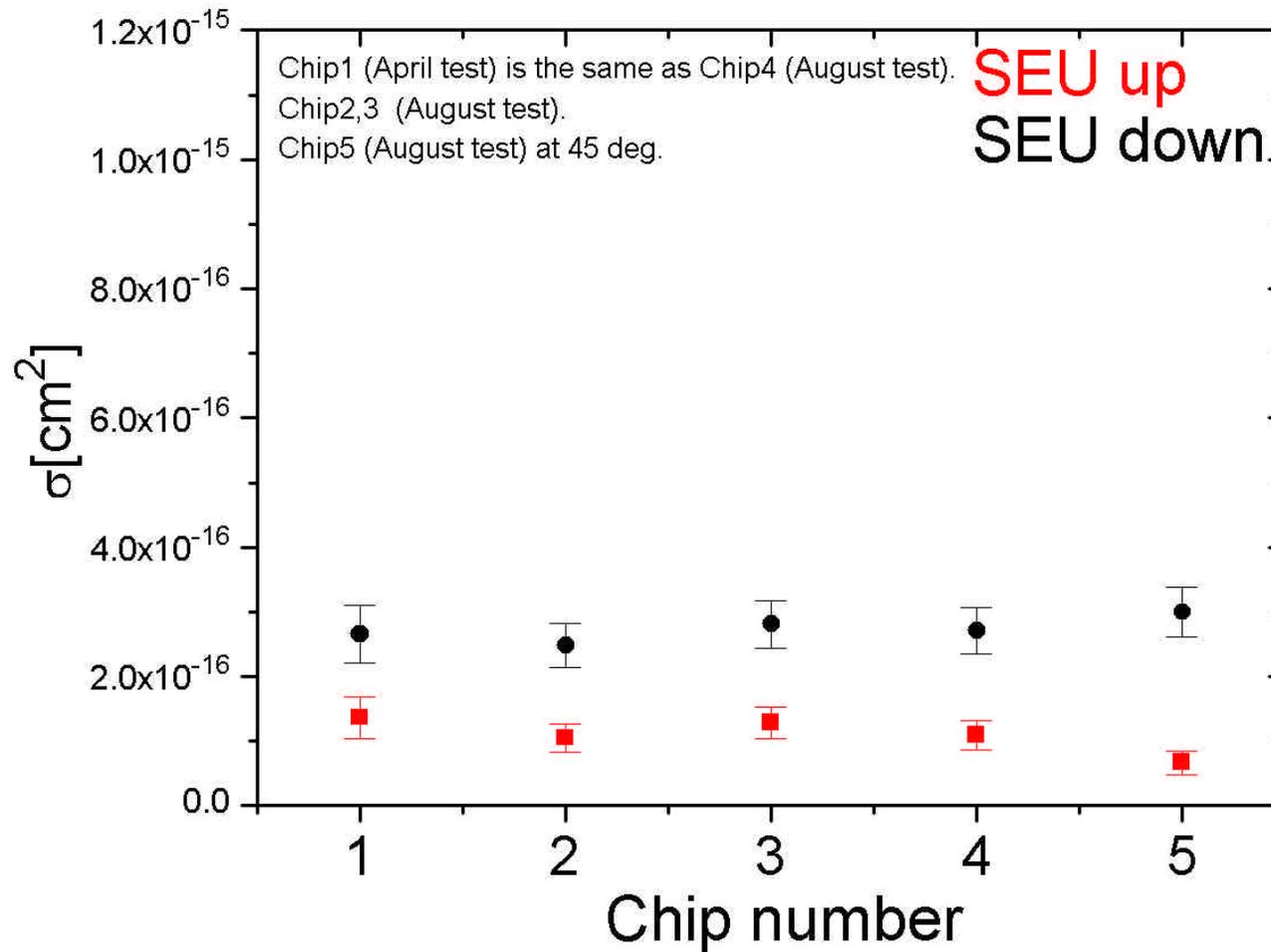
Test	Board	Integrated fluence [cm <sup>-2</sup> ]	Bit errors	Bit errors in s-r	Bit errors in DAC
April	1	2.33E14	63	53=18↑+35↓	10=8↑+2↓
August	2	3.65E14	93	74=22↑+52↓	19=9↑+10↓
August	3	3.65E14	105	86=27↑+59↓	19=8↑+11↓
August	4	3.65E14	100	80=23↑+57↓	20=8↑+12↓
August	5	3.65E14	108	77=14↑+63↓	31=19↑+12↓

N.B. The SR's were downloaded with equal number of 0's and 1's but the DAC's with 57 0's and 55 1's.

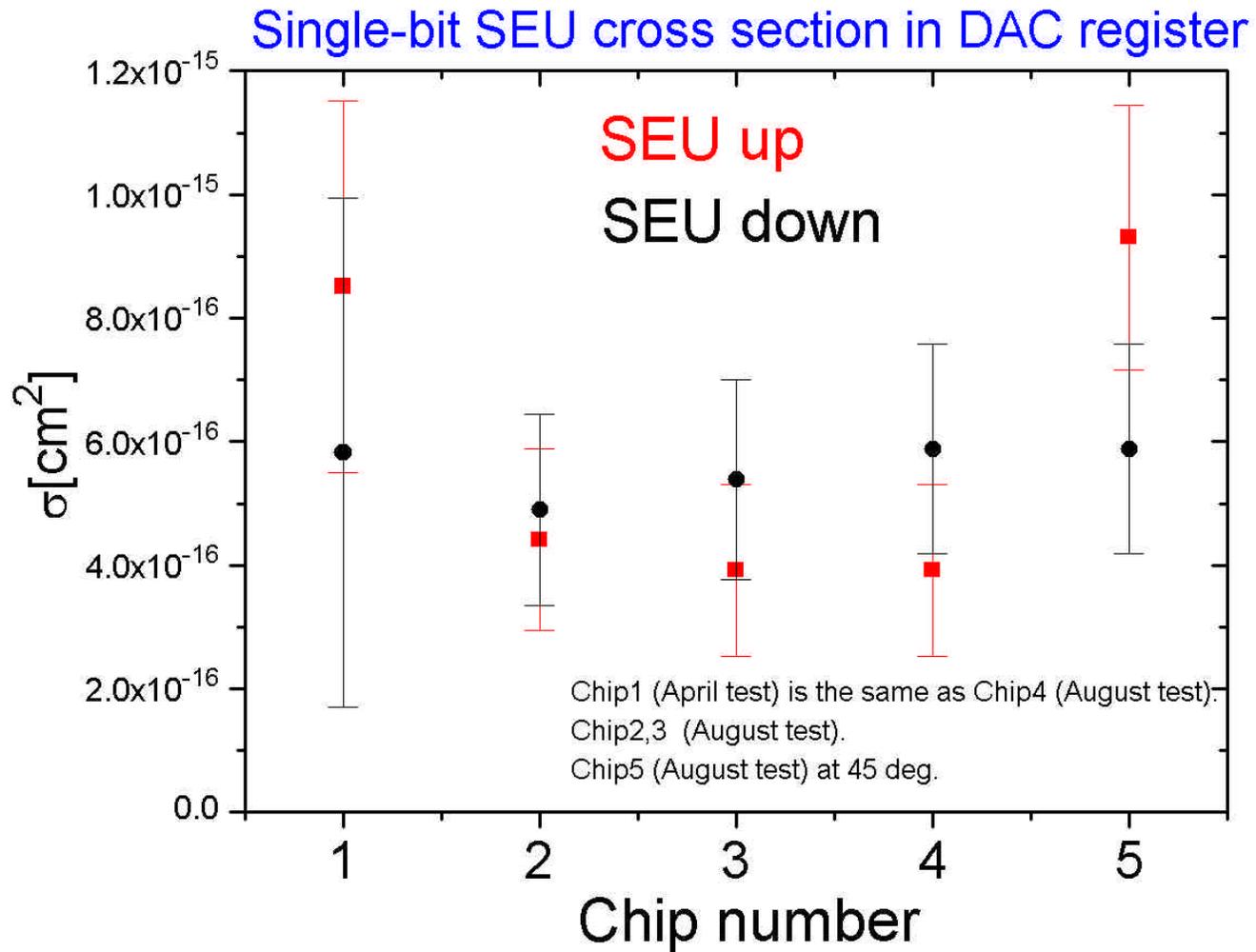
- =transition from 0 to 1  
- =transition from 1 to 0

# Results: Shift register

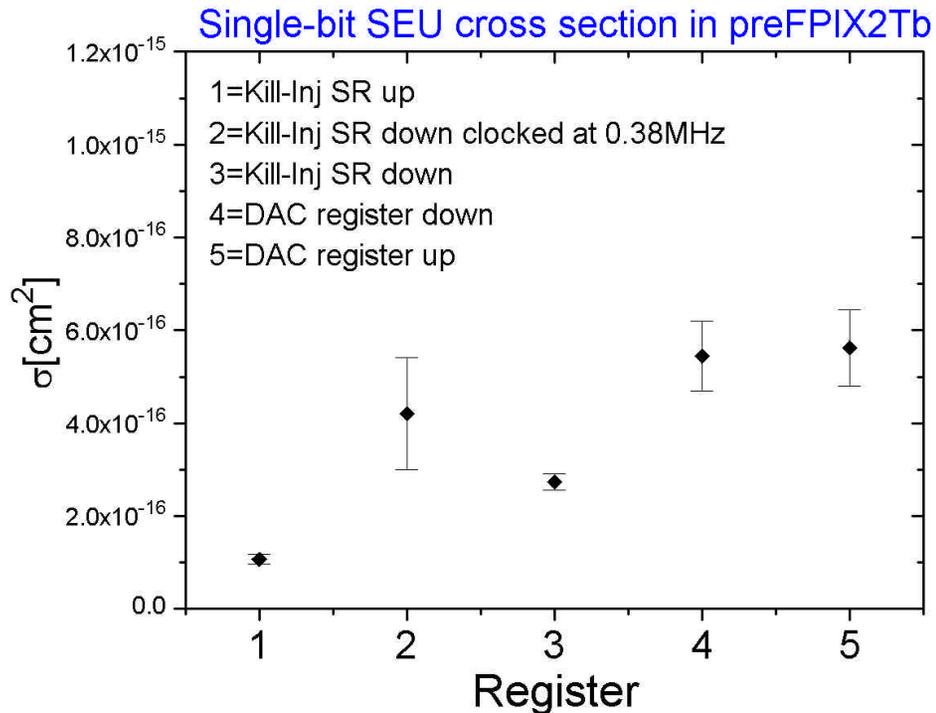
Single-bit SEU cross section in Kill-Inj shift register



# Results: DAC register



# Results: summary



N.B. the uncertainty in the integrated fluence is less than 10%

April 01 + Aug 01

April 01

$$S_{SEU,SR}^{0 \rightarrow 1} = (1.3 \pm 0.3) \cdot 10^{-16} cm^2$$

$$S_{SEU,SR}^{1 \rightarrow 0} = (2.6 \pm 0.5) \cdot 10^{-16} cm^2$$

$$S_{SEU,DAC} = (3.8 \pm 1.2) \cdot 10^{-16} cm^2$$

$$S_{SEU,SR}^{0 \rightarrow 1} = (1.0 \pm 0.1) \cdot 10^{-16} cm^2$$

$$S_{SEU,SR}^{1 \rightarrow 0} = (2.7 \pm 0.7) \cdot 10^{-16} cm^2$$

$$S_{SEU,SR,clocked}^{1 \rightarrow 0} = (4.2 \pm 1.2) \cdot 10^{-16} cm^2$$

$$S_{SEU,DAC} = (5.5 \pm 0.6) \cdot 10^{-16} cm^2$$

# Estimated error rate in BTeV

## Formulas

$$N_{\text{bit error}} = N_{\text{plane}} \mathbf{r}_{\text{bit}} \text{BeamGap} \sum_k \int \frac{d\text{Flux}_k(E, r)}{dE} \cdot \mathbf{S}_{k, \text{one bit}}(E) dE dx dy$$

Beam gap BG temporal structure of 99/159=0.62

$$\mathbf{r}_{\text{kill-bit}} = \frac{1}{50 \cdot 400 \text{mm}^2} = 5000 \frac{\text{pixel}}{\text{cm}^2} = 5000 \frac{\text{kill-bit}}{\text{cm}^2}$$

$$\mathbf{r}_{\text{DAC-bit}} = \frac{N_{\text{bit in DAC}} N_{\text{DAC}}}{N_{\text{cells per chip}}} \mathbf{r}_{\text{kill-bit}} = 199 \frac{\text{DAC-bit}}{\text{cm}^2}$$

$$\mathbf{r}_{\text{Ser-bit}} = \frac{N_{\text{bit in Ser}}}{N_{\text{cells per chip}}} \mathbf{r}_{\text{kill-bit}} = 44 \frac{\text{Ser-bit}}{\text{cm}^2} \quad \begin{array}{l} \underline{\text{Assumed}} \\ \underline{24 \text{ bit serializer}} \end{array}$$

# Estimated error rate in BTeV

Flux from Mars simulation ( $L=2E32\text{cm}^{-2}\text{s}^{-1}$ )

Radius [cm]	<Ch.Hadrons> ( $E>10\text{MeV}$ ) [Hz/cm <sup>2</sup> ]	<Neutrons> ( $E>14\text{MeV}$ ) [Hz/cm <sup>2</sup> ]	<Neutrons> ( $E<14\text{MeV}$ ) [Hz/cm <sup>2</sup> ]	<elects> and <g> ( $E>100\text{KeV}$ ) [Hz/cm <sup>2</sup> ]
0.6-2	6.4E6	7.2E5	2.5E5	1E6 and 6E6
2-3	2E6	3E5	1.8E5	4E5 and 2E6
3-4	9E5	1.7E5	1.5E5	2.3E5 and 1E6
4-5	5E5	9.4E4	1.3E5	1.5E5 and 6E5
5-6	3E5	7E4	1.2E5	9E4 and 4.8E5
6-7	2E5	5E4	1E5	7E4 and 4.9E5
<b>Flux per plane [Hz]</b>	<b>1.4E8</b>	<b>0.15E8</b>	<b>0.20E8</b>	-
<b>SRkill[seu/h]</b>	<b>10</b>	<b>1*HN</b>	<b>1.4*LN</b>	-
<b>DAC [seu/h]</b>	<b>2</b>	<b>0.2*HN</b>	<b>0.3*LN</b>	-
<b>Ser [seu/h]</b>	<b>1*clock</b>	<b>0.09*clock*HN</b>	<b>0.1*clock*LN</b>	-

# Conclusions

- We measured SEU's in preFPIX2Tb with a rate similar to what reported from other collaborations.
- The test done in April with one chip is consistent with the test done in August with 4 chips.
- No significant variation in the SEU cross section rate between different chips.
- For the kill and Inj mask shift-register the bit upset from 0 to 1 as a smaller cross section than 1 from 0. Expected from the layout.

# Next

- Irradiate detectors (September 01).
- Understand SEU cross-section and Flux of epithermal neutron ( $E < 1\text{eV}$ ).
- Further SEU's tests in shift register with clocked mode at high frequency (1-30 MHz).
  - » We need the mezzanine card to generate high frequency clock.
- Look one more time from the circuit point of view if SEU phenomena can freeze the readout chip or part of it.
  - » Flip-Flop's and State machines
  - » Unit cell
  - » End Of Column
  - » Peripheral data serializer
  - » ...