



<http://ectc.net>

- **51st ECTC: over 250 technical papers in 38 sessions**
- **Largest Packaging Conference in the World**
- **Fermilab's paper presentation attended by ~100 people**

- **Advanced Packaging**
- **Modeling & Simulation**
- **Optoelectronics**
- **Interconnections**
- **Materials & Processing**
- **Quality & Reliability**
- **Manufacturing Technology**
- **Components & RF**
- **Connectors & Contacts**
- **Education**
- **Poster**

Big players were there...

Georgia Tech (PRC): 35 papers

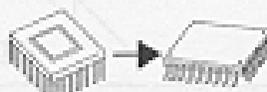
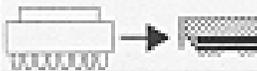
IBM: 13 papers

Intel: 9 papers

Motorola: 14 papers

Lucent, Alcatel, Compaq, Boeing, Xerox, Altera, HP, Honeywell, Rockwell, Nokia, NTT, Philips, Siemens, Samsung, TI, Tyco ...

Packaging Evolution

	1970's	1980's	1990's	Next Need
	DIP	PGA QFP	BGA CSP	Water-Level Packaging with SOC/SOP
Single Chip:				
Chip Connector:	Wirebond	Redistribution to Area Array	Flipchip Area Array	
Board MCM:	Ceramic	Ceramic or Thin Film on Ceramic	Thin Film on PWB	
Board:	PWB-D	PWB-D	PWB-Micro Via	
Board Connector:	PTH	Peripheral SMT	Area/BGA SMT	
Discretes:	1005	0805 → 0603	0402	
				<ul style="list-style-type: none"> • High-Speed Digital • High Band-Width Optical • RF • Analog • MEMS

Flip Chip: Worldwide Perspectives

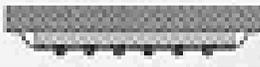
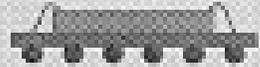
- **Personal computers** set the trends for packaging in the 1990's
 - Intel sets the trends
 - All new CPU's are flip chip designs
 - AMD
 - Flip chip ceramic substrate
 - Motorola
 - Flip chip on ceramic substrates

Flip Chip: Worldwide Perspectives

- **Game Machines: Driver for the Next Decade**
 - Sony PlayStation 2
 - Emotion Engine integrates **13.5 M transistors** (>Pentium III!)
 - Package in 42.5x42.5mm with 540 solder balls
 - System sells for ~ **US\$350!!**

Games will evolve into home computer/internet appliance of the future

Chip Scale Packages Worldwide

Category	Type	Example	Devices	Applications
Flex Interposer	TAB/flip chip		Flash, SRAM, ASIC, Microcontroller, DSP	Camcorder, cell phone, memory card, computer
	Wire bonding			
Rigid Substrate	Flip chip		Processor, Controller, DSP, SRAM, ASIC	Cell phone, camcorder, PDA
	Wire bonding			
Lead Frame	Wire bonding		Flash, DRAM, analog IC	Cell phone, memory card, notebook
Water-Level Assembly	Redistribution		Memory, controllers, ASICs, sensors, op-amp, power devices	Computers, communications
	Substrate			

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Source: TechSearch International, Inc.

Strategic IC Roadmap

	1992	1995	1998	2001	2005	2008
Feature size (μm)	0.5	0.35	0.25	0.18	0.12	0.07
Transistors/(cm^2)	0.01B	0.04B	0.1B	0.22B	0.88B	2.5B
Chip size (mm^2)						
-logic/uniprocessor	250	400	600	800	1000	800
-DRAM	132	200	320	500	526	603
Maximum power (W/die)						
-high performance	10	15	30	115	150	170
-portable	3	4	4	1.7	2.4	2
Power supply voltage (V)						
-desktop	5	3.3	2.2	1.8	0.9	0.9
-portable	3.3	2.2	2.2	1.8	0.9	0.6
No. I/Os	500	750	1500	2000	3800	4600

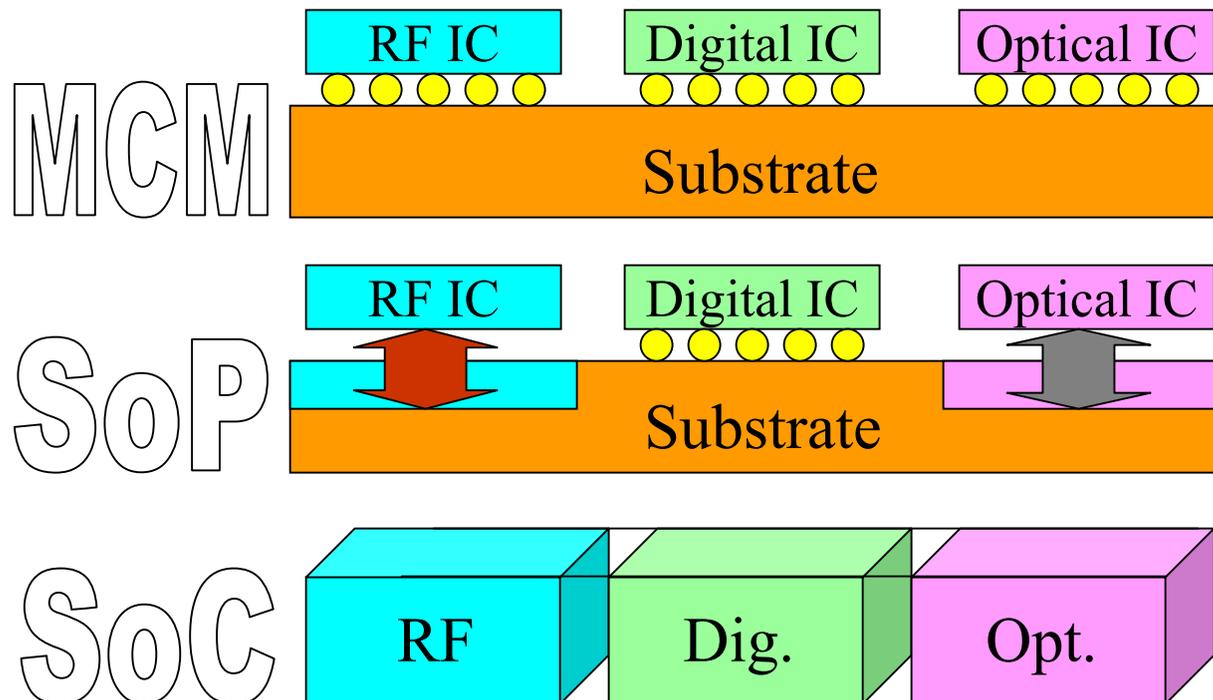
Strategic IC Roadmap

High Density Wiring Need!

Substrate Lines and Spaces (microns)	2001	2003	2005	2011
Hand Held (6 layer, or 4 layer with microvia)	60	35	30	20
Cost Performance (4 or 6 layer)	125	100	75	75
High Performance (laminate)	55/75	55/75	50/70	35/55
High Performance (thin film)	10/20	8/16	6/12	5/10
Automotive (6 layer w/microvia)	100	100	75	25
Military (10 layer)	75	75	50/75	50

General Discussion: SoP or SoC?

- Motivation: **Package density increasing, new solutions necessary!**
- **Japan** has been working on SoC for a long time. No success so far.
- SoP is the answer from **USA** for the future.
- **Europe** is waiting to see what comes out the discussion. Groups working in both approaches



Some Technical Points (USA & ½ Europe)

SoC

- Difficulty in capturing system design domains (RF, digital, opto...)
- Lack of co-design methods and tools
- Limited performance obtained from RF components
- Difficulty in heterogeneous integration
- Lack of verification and test tools and technologies for SOCs
- Manufacturing and yield related problems for large ICs

SoP

- Existing design methods can be used
- Interconnect functionality can be transferred from IC onto substrate
- Higher performance RF functions can be included in the SoP
- Better isolation between RF, analog, and digital components (**coupling through substrate to be solved**)
- Passive components can be integrated within package

Further reading: **SoC or SoP? A Balanced Approach!**, Evan Davidson - IBM Corporation

Neat Technologies... Bump-less Interconnect

- Metals: Al, Cu, Ag, Au, Sn, In, Ti, Ni and their alloys
- Combinations to ceramics or semiconductor: SiC, Si₃N₄, Al₂O₃, AlN, diamond and silicon
- Heterojunctions: Si-GaAs, Si-InP, and GaAs-InP

Argon fast atom beams (FAB) of about 1.5 kV power source are used, instead of ion beams. The bonding is achieved only by contact at a room temperature.

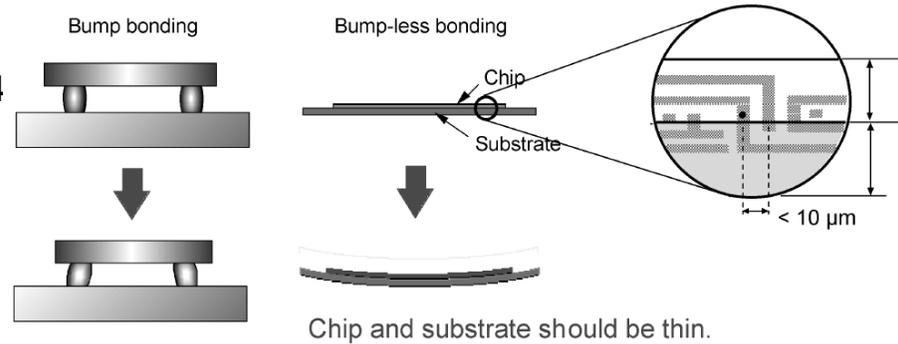


Figure 3. Reduction of CTE mismatch in case of bump-less interconnect.

At least, Au and Au are bonded successfully without any difficulty in atmospheric pressure of N₂ or Ar, whereas Cu loses the surface activity slowly, and Al extremely fast, so that Al can be bonded only in vacuum.

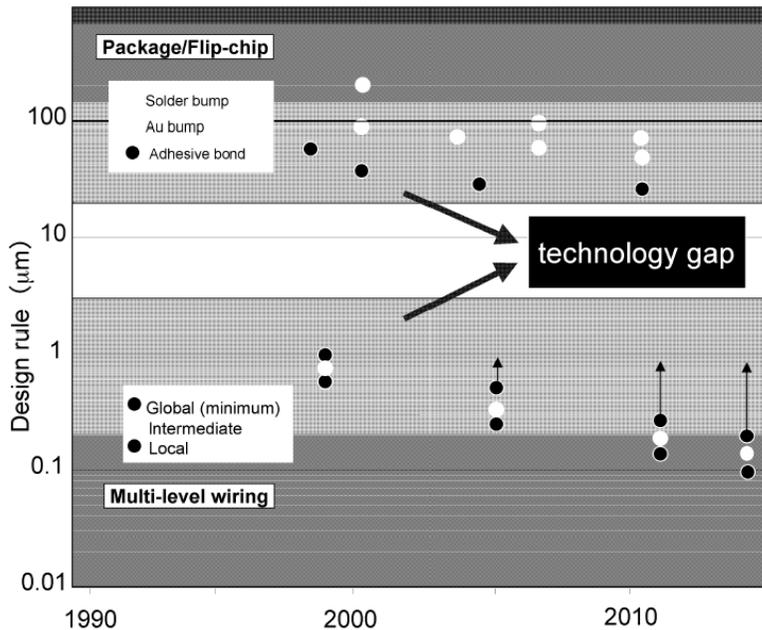


Figure 1. Technology gap in the design rule between on-chip wiring and packaging interconnects.

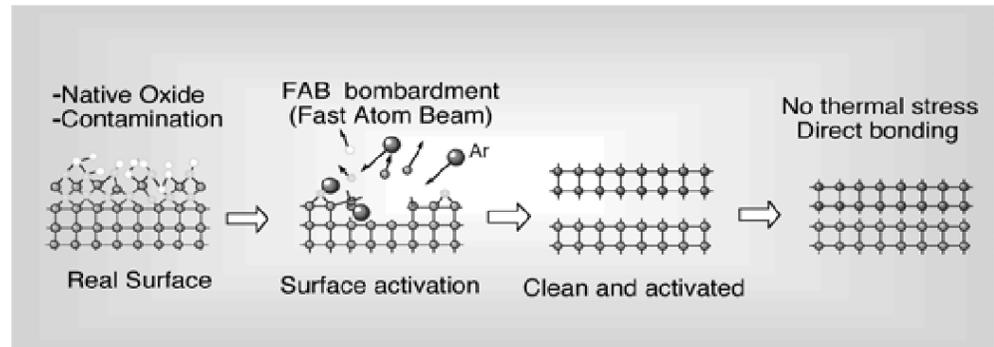


Figure 6. Concept of surface activated bonding

Neat Technologies...Sharp's Stacked CSP

