FPIX1 Pad Description

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Pad List

Pad #	Pad #	Pad Name	Brief Description
1		Vssa	- Substrate voltage and ground for pixel analog circuitry (0V)
	2	Inject In	- Analog Input for test charge
3		Vdda	- Power for pixel analog circuitry (3.3V)
	4	Ivbbnl	- Decoupling point and override for internal bias
5		Vss_comp	- Ground for pixel A to D conversion (0V)
	6	Ivfb	- Feedback current (decoupled)
7		Vdd_comp	- Power for pixel A to D conversion (3.3V)
	8	Ivbbp	- Master Bias Current (decoupled)
9		Vssd	- Ground for pixel command interpreter and drivers (0V)
	10	Ivbbn	- Decoupling point and override for internal bias
11		Vddd	- Power for pixel command interpreter and drivers (3.3V)
	12	Ivbbpl	- Decoupling point and override for internal bias
13		Vsub	- Substrate voltage (0 V)
	14	Ivbb_comp	- Decoupling point and override for internal bias
15		Vssd_eoc	- Ground for End-of-column Logic (0V)
	16	Vth3	- Most significant threshold for ADC
17		Vddd_eoc	- Power for End-of-column Logic (3.3V)
	18	Vth2	- Threshold for ADC

19		Vsub	- Substrate voltage (0V)
	20	Vth1	- Threshold for ADC
21		Vssd_eoc	- Ground for End-of-column Logic (0V)
	22	Vth0	- Threshold for Hit Comparator
23		Vddd_eoc	- Power for End-of-column Logic (3.3V)
	24	Vpstop	- Bias voltage for the detector p-stops
25		Vsub	- Substrate voltage(0V)
	26	Vnguard	- Bias for the detector n-guard
27		TokenIn	
	28	TokenIn*	- Input for the chip token
29		TrigAcc	- Under triggered mode, the trigger signal; Under non-triggered mode, the throttle (3.3V = Accept)
	30	ShiftIn	- Input for the scan paths
31		DataReset	- Reset signal which clears all clock, counter and data registers
	32	ProgramRes	- Reset signal which clears all scan paths except Kill and Inject
33		ShClk	- Shift Clock signal
	34	ReadClk*	
35		ReadClk	- The Readout Clock
	36	BCOClk*	
37		BCOClk	- The Beam Cross Over clock
	38	Data0*	

39		Data0	- Row 0 or RBC0 0 (LVDS levels)
	40	Data1*	
41		Data1	- Row 1 or RBC0 1 (LVDS levels)
	42	Data2*	
43		Data2	- Row 2 or RBC0 2 (LVDS levels)
	44	Data3*	
45		Data3	- Row 3 or RBC0 3 (LVDS levels)
	46	Data4*	
47		Data4	- Row 4 or RBC0 4 (LVDS levels)
	48	Data5*	
49		Data5	- Row 5 or RBC0 5 (MSB RBC0) (LVDS levels)
	50	LoadKill	- On the falling edge of this signal the Kill pattern is loaded into the pixels
51		Vss_pad	- Ground for the pad circuitry (0V)
	52	ChipHasData	- Diagnostic pad using CMOS levels (high if chip has data)
53		Vdd_pad	- Power for pad circuitry (3.3V)
	54	Data6*	
55		Data6	- Row 6 or Logic 0 (LVDS levels)
	56	Data7*	
57		Data7	- Row 7 (MSB Row Address) or Logic 0 (LVDS levels)
	58	Data8*	
59		Data8	- Col 0 or ChipID 0 (LVDS levels)

	60	Data9*	
61		Data9	- Col 1 or ChipID 1 (LVDS levels)
	62	Data10*	
63		Data10	- Col 2 or ChipID 2 (LVDS levels)
	64	Data11*	
65		Data11	- Col 3 or ChipID 3 (MSB ChipID) (LVDS levels)
	66	Data12*	
67		Data12	- Col 4 (MSB Col Addr) or Logic 0 (LVDS levels)
	68	Data13*	
69		Data13	- ADC0 or Logic 0 (LVDS levels)
	70	Data14*	
71		Data14	- ADC1 (MSB ADC) or Logic0 (LVDS levels)
	72	Data15*	
73		Data15	- Logic 1 (Data) or Logic 0 (Control) (LVDS levels)
	74	Data16	
75		Data16*	- Data Valid
	76	Reg2	- Scan path selection (MSB)
77		Vddd	- Power for pixel command interpreter and drivers (3.3V)
	78	Reg1	- Scan path selection bit
79		Vssd	- Ground for pixel command interpreter and drivers (0V)
	80	Reg0	- Scan path selection bit
81		Vss_comp	- Ground for pixel A to D conversion (0V)

	82	Shift Out	- Output from scan path
83		Vdd_comp	- Power for pixel A to D conversion (3.3V)
	84	TokenOut*	
85		Vdda	- Power for pixel analog circuitry (3.3V)
	86	Token Out	Chip Token Output
87		Vssa	Substrate Voltage and ground for pixel analog circuitry (3.3V)

Detailed Pad Description

1. **Vssa**: Analog ground. Tie directly to a low impedance, low-noise ground plane

2. **Inject-In**: This is the analog test input. Pixels are set for Injection and/or Killed by the Kill/Inject scan path. Those, which are set for Injection and not Killed, are given a charge through Inject-In. This pin is generally tied to analog ground through a 50-ohm resistor. A voltage pulse on this pin causes charge injection into the appropriate pixels. The magnitude of this injection is a function of the size of the voltage pulse. As the design is optimized for electron collection, the charge is injected on the negative edge of the pulse. If you are NOT injecting, keep this pad at an AC ground. If you are injecting, start the signal at X volts, drop it to some voltage less than X volts, and hold it at this new voltage. X is greater than 1 volt and less than 2 volts

3. **Vdda**: Analog VDD = 3.3V. A ±10% variation on this voltage has been allowed for by simulation. However, users should nevertheless consider 3.3 volts a religious obligation. Board designers should design this trace to handle a sustained DC current of approximately 100 mA.

4. **Ivbbnl**: 1 nF decoupling capacitor to analog ground. This pad may be optionally used for optimization

5. **Vss_comp**: Ground for analog to digital converters in each pixel. It should be tied to the same low impedance, low-noise ground plane as Vssa (pad 1)

6. **Ivfb**: 1 nF decoupling capacitor to analog ground. 5 nA (nominal) current should be sunk from the chip.

7. **Vdd_comp**: VDD for analog to digital converters. 3.3 Volts

8. **Ivbbp**: 1 nF decoupling capacitor to analog ground. 7 μA (nominal) current should be sunk from the chip.

9. **Vssd**: Digital Ground for digital circuitry in the pixel cells. This should be connected to a low impedance, "dirty" ground plane. It should NOT be connected to the analog ground plane.

10. **Ivbbn**: 1 nF decoupling capacitor to analog ground. This pad may be optionally used for optimization.

11. **Vddd**: Digital Power for digital circuitry in the pixel cells. 3.3 volts. It is also "dirty" and should NOT be connected to analog power. It should also be able to handle a sustained DC current of approximately 100 mA.

12. **Ivbbpl**: 1 nF decoupling capacitor to analog ground. This pad may be optionally used for optimization.

13. **Vsub**: Substrate voltage (0 V). It should be connected to the low impedance, low noise analog ground plane. DC current consumption should be 0 amps.

14. **Ivbb_comp**: 1 nF decoupling capacitor to analog ground. This pad may be optionally used for optimization.

15. **Vssd_eoc**: Digital Ground for the End-of-column circuitry. 0V. This should be connected to a low impedance, "dirty" ground plane. It should NOT be connected to the analog ground plane.

16. **Vth3**: Threshold voltage for the most significant analog to digital comparator. 2V – 0V.

17. **Vddd_eoc**: Digital Power for End-of-column circuitry. 3.3V. It is also "dirty" and should NOT be connected to analog power.

18. **Vth2**: Threshold voltage for the "middle" analog to digital comparator. 2V – 0V.

19. **Vsub**: Substrate voltage (0 V). It should be connected to the low impedance, low noise analog ground plane.

20. **Vth1**: Threshold voltage for the least significant analog to digital comparator. 2V – 0V.

21. **Vssd_eoc**: Digital Ground for the End-of-column circuitry. 0V. This should be connected to a low impedance, "dirty" ground plane. It should NOT be connected to the analog ground plane.

22. **Vth0**: Threshold voltage for the Hit comparator. 2V – 0V.

23. **Vddd_eoc**: Digital Power for End-of-column circuitry. 3.3V. It is also "dirty" and should NOT be connected to analog power.

24. **Vpstop**: Detector bias. This voltage is dependent on which detector is used

25. **Vsub**: Substrate voltage (0 V). It should be connected to the low impedance, low noise analog ground plane.

26. **Vnguard**: Detector bias. This voltage is dependent on which detector is used

27-28: **Token In/Token In***: Low voltage differential signal input (Vhi ≅ 1.75V; Vlo ≅ 1.55V). When this signal is high (Pad 27 = 1.75V; Pad 28 = 1.55V), the chip can take the bus. When this signal is low (Pad 27 = 1.55V; Pad 28 = 1.75V), the chip cannot take the bus and its data outputs are tri-stated. This is the only LVDS input that has its own internal 100-ohm load resistor. This signal can be held high for the hottest chip.

29. **TrigAcc**: TrigAcc is a dual-mode signal. When the chip is operating in Triggered mode, it is the trigger signal, and on the rising edge of this signal, the requested BCO number is replaced by the Trigger most recently scanned into the chip. When the chip is operating in Non-triggered or continuous mode, it is the Accept/Reject signal. When Accept/Reject is a logical high (3.3 volts), the chip accepts incoming data. When Accept/Reject is a logical low (0 volts), the chip rejects (ignores) incoming data. In either mode, this is a single ended CMOS signal.

30. **ShiftIn**: CMOS input for the scan paths. At the rising edge of the ShiftClk, the value at the shift in will be scanned into the path chosen by the Reg0, Reg1, and Reg2 signals.

31. **DataReset**; CMOS level reset signal. When high (3.3 volts), the BCO counters are reset to zero; the End-of-column registers are reset to Empty; the chip stops Talking.

32. **ProgramReset**: CMOS level reset signal. When high (3.3 volts), the mask registers are reset to zero (no masking); the chip is reset to continuous mode (Non-triggered); the BCO lag is set to 2; the ChipID is set to zero.

33. **ShClk**: The Shift Clock is a CMOS level clock. At the rising edge of this clock, the contents of the ShiftIn are scanned into whatever scan path is selected by Reg<0:2>.

34-35. **ReadClk*/ReadClk:** A free-running LVDS level differential clock (Vhi=1.75V; Vlow=1.55V). The simulated frequency was 26 MHz, but the real frequency will be whatever the chip can handle and/or whatever the board can supply.

36-37: **BCOClk*/BCOClk:** This is an LVDS representation of the Beam Crossover signal.

38-49; 54-75: **DATA:** These are the data outputs. They are tri-statable LVDS outputs (Vhi=1.75V; Vlow=1.55V) with the exception of Data 16. Data 16 is the Data Valid signal. It is a tri-statable LVDS IO, which senses the present state of the Data Valid and reacts to that state depending on whether or not the chip has data to send. In the following table, Data 16 is shown as being 0 if no data is available. This is because if the chip is alone, it will never tri-state its Data Valid signal. If the chip is part of a Daisy Chain, then there will always be one chip driving the Data Valid signal. Therefore, a user should never really see Data Valid in a high impedance state. When there is data available, Data Valid will be a 1. When there is data available, it will come in two forms: Control Words which tell the data acquisition system the chip ID of the chip sending the data and BCO number (time stamp) of the data; and Data Words which tell the Row Address, Column Address and Magnitude (ADC value) of a particular hit pixel. Control Words are

distinguished from Data Words by bit Data 15, which is a Logical 0 for a Control Word and a Logical 1 for a Data Word.

	No Data Available	*Data Available Control Word*	*Data Available Data Word*
Data 16/Data 16*	0	Logical 1	Logical 1
Data 15/Data 15*	X	Logical 0	Logical 1
Data 14/Data 14*	X	Logical 0	ADC [1]
Data 13/Data 13*	X	Logical 0	ADC [0]
Data 12/Data 12*	X	Logical 0	Col Addr[4]
Data 11/Data 11*	X	ChipID [0]	Col Addr[3]
Data 10/Data 10*	X	ChipID [0]	Col Addr[2]
Data 9/Data 9*	X	ChipID [0]	Col Addr[1]
Data 8/Data 8*	X	ChipID [0]	Col Addr[0]
Data 7/Data 7*	X	Logical 0	Row Addr[7]
Data 6/Data 6*	X	Logical 0	Row Addr[6]
Data 5/Data 5*	X	BCO[5]	Row Addr[5]
Data 4/Data 4*	X	BCO[4]	Row Addr[4]
Data 3/Data 3*	X	BCO[3]	Row Addr[3]
Data 2/Data 2*	X	BCO[2]	Row Addr[2]
Data 1/Data 1*	X	BCO[1]	Row Addr[1]
Data 0/Data 0*	X	BCO[0]	Row Addr[0]

50. **Load Kill**: The falling edge of this signal latches the kill pattern scanned into the pixel array. It is a CMOS level signal which is kept at a Logical 1 (3.3 volts) during the Kill scan and dropped to a Logical 0 to latch the kill pattern. During normal operation, it is kept at a Logical 0.

51. **Vss_pad**: Ground for the pad circuitry. 0V. This should be connected to a low impedance, "dirty" ground plane. It should NOT be connected to the analog ground plane.

52. **ChipHasData**: This is a CMOS level diagnostic output which goes to a Logical 1 when the chip has data to output in response to the current requested BCO number.

53. **Vdd_pad**: Power for the pad circuitry. 3.3V. It is also "dirty" and should NOT be connected to analog power. The board designer should expect that this signal will carry 50 mA and it will turn on when the chip has data to output and turn off when the chip tri-states itself.

76, 78, 80: **Reg<2:0>**: The scan path selectors for the ShiftIn. These are CMOS inputs and they should be set to 000 during normal, continuous mode operation. They will likely be set to 001 during normal, triggered mode operation.

77. **Vddd**: Digital Power for digital circuitry in the pixel cells. 3.3 volts. It is also "dirty" and should NOT be connected to analog power. It should also be able to handle a sustained DC current of approximately 100 mA.

79. **Vssd:** Digital Ground for digital circuitry in the pixel cells. This should be connected to a low impedance, "dirty" ground plane. It should NOT be connected to the analog ground plane.

81. **Vss_comp**: Ground for analog to digital converters in each pixel. It should be tied to the same low impedance, low-noise ground plane as Vssa (pad 1)

82. **ShiftOut**: The scan output for each of the scan paths as selected by Reg<2:0>. This is a CMOS level signal, which will be driven to the ShiftIn of the next chip.

83. **Vdd_comp**: VDD for analog to digital converters. 3.3 Volts

84,86. **TokenOut*/TokenOut**: The LVDS output of the Chip Token signal (Vhi=1.75V; Vlow=1.55V). Unlike the Data outputs, this is not tri-statable.

85. **Vdda**: Analog VDD = 3.3V. A ±10% variation on this voltage has been allowed for by simulation. However, users should nevertheless consider 3.3 volts a religious obligation. Board designers should design this trace to handle a sustained DC current of approximately 100 mA.

87. **Vssa**: Analog ground. Tie directly to a low impedance, low-noise ground plane

All LVDS outputs with the exception of the TokenOut will require a 100-ohm load impedance. TokenOut does not require this because the load is included in the TokenIn pad circuitry. The LVDS receivers for the ReadClk and the BCOClk will, likewise require a 100-ohm load impedance. The CMOS outs and ins require no special circuitry.

Programming and the Scan Paths

There are eight internal scan paths in FPIX1. Each scan path uses the same ShiftIn, the same Shift Out and the same ShClk. The particular scan path chosen is

determined by the bit code set onto pads 76, 78 and 80 also known as Reg[2:0]. The paths are as follows:

	Bit Pattern	Path
0	000	Idle – no path
1	001	Trigger path
2	010	Not used
3	011	Mask registers
4	100	Not used
5	101	Mode, ChipID and Lag
6	110	Kill or Inject
7	111	Kill or Inject

The Idle path should be the default path. If nothing is happening, Reg[2:0] should be set to 000. Paths 010 or 100 are, for the moment, the same as Path 000. However, in the future (FPIX2, etc) it is likely that they will be used for diagnostic scan paths or D-to-A converter scan paths.

The Trigger path (001) is used when the chip is in External Trigger Mode. It is a six bit deep path and the most significant bit should be scanned in first. When all six bits have been scanned in, a pulse on the TrigAcc pin (pad 29) will cause the new requested trigger to be presented to the End-of-column Logic cells. Using this scan path in Continuous Mode will have no effect.

The Mask register path (011) is used to set the programmable reset delay. Each end of column logic has a six bit deep Mask register. A Logic 1 located in any bit of

this register causes the comparison between the Current BCO number and the Stored BCO number to be ignored. Since the End-of-column Set sends a reset command when the Current BCO number equals the Stored BCO number, the presence of the mask register allows the user to decide how long data is stored before it is reset. With all the bits in the mask register equal to zero, the End-of-column Set will reset itself in 64 BCO clock cycles. With the most significant bit ignored, the End-of-column Set will reset itself in 32 clock cycles. With all bits in the mask register set to one, the column is effectively shut down. With six bits per End-of-column cell, this scan path has 6 x 17 = 102 bits. The most significant bit of column 17 is scanned in first. The least significant bit of column 1 is scanned in last.

The Mode path (101) is probably the most important path in the chip. It contains the chip Mode (1=Triggered Mode, 0=Continuous Mode), the Chip ID, and the BCO lag. The BCO lag is the minimum distance between the current BCO number and the requested BCO number in Continuous Mode. Typically, this number is set to two so that if, for example, the current BCO number was 5, the maximum value of the requested BCO number would be 3. With 6 bits for the lag, 4 bits for the ChipID and 1 bit for the mode, this scan path is 11 bits long. The most significant bit of the lag is scanned in first followed by the remainder of the lag. Then the most significant bit of the ChipID is scanned in followed by the remainder of the ChipID. Finally, the mode is scanned in.

Of virtually equal importance to the Mode path is the Kill/Inject path (110 or 111). It is 160x18x2=5760 bits long. The first 2880 bits is the Kill and the second 2880 bits is the Inject. During the Kill, LoadKill (pad 50) is held high. It is dropped low before the first bit of the Inject is scanned in. The scan path starts at the lowest pixel of the 17^{th} column and proceeds up the column to the highest pixel. From there, the path moves to the highest pixel in the 16^{th} column and proceeds from

there to the lowest pixel. In other words, if it is an odd numbered column, the path receives its input at the lowest pixel from the column to its right and scans the data to the highest pixel of this odd numbered column where it outputs the path to the column on its left. If it is an even numbered column, the path receives its input at the highest pixel from the column to its right and scans the data to the lowest pixel of this even numbered column where it outputs the path to the column to its left. For example, in a 4x4 pixel FPIX1, the pixels, in reality, would be numbered as follows:

3	3	3	3
2	2	2	2
1	1	1	1
0	0	0	0

However, to the scan path, they appear like this:.

13	12	5	4
14	11	6	3
15	10	7	2
16	9	8	1

A Logical 1 in the Kill pattern means that the pixel is killed. A Logical 0 in the Inject pattern means that the pixel will be injected.

During all scanning operations in Continuous Mode, the TrigAcc signal (pad 29) should be held to a Logical 0 (reject). This is a precaution to prevent accidental injection of hits. If possible, DataReset should be activated after programming is done and before TrigAcc is returned to a Logical 1 (accepts). In External Trigger Mode, it is impossible to use TrigAcc in this way. However, since the Trigger path is far away from the Pixels, there should be no problem with accidental hits.

All of the Scan Signals (ShClk, ShiftIn, Shift Out, Reg[2:0] and TrigAcc) are all single-ended CMOS-level signals.

Data and Data Valid

Data Valid (pads 74 and 75) is high (pad 74 higher in voltage than pad 75) when there is data being driven on the bus and low (pad 74 lower in voltage than pad 75) when there is no data on the bus. Data will be changed at the falling edge of the ReadClk and will be stable at the rising edge of the ReadClk. Therefore, Data should be latched by the DAQ system at the rising edge of the ReadClk when Data Valid is high.

DataX is the "true" version of the differential signal. DataX* is the "bar" version. When DataX is higher in voltage than DataX*, the bit is a logical 1.

Token Passing

FPIX1 was meant to be Daisy-chained. Token Out is placed such that it can be fed straight into the Token In of the next chip in the chain. Token In is the only LVDS input to have its own internal load resistor.

If the chip is to be used in a single chip mode, its Token In can be set to a logical 1. In this case, its Token Out will be a square wave at on half the ReadClk frequency.

Resetting

Pulsing Program Reset (Pad 32) will do the following:

1. The External Trigger will be reset to zero.

2. Every Mask register in every column will be restored to all zeros. In other words, the End-of-column Sets will reset themselves 64 clock cycles after they have been hit.

3. The chip will be reset to Continuous Mode

4. The ChipID will be reset to 0000.

5. The lag will be reset to 2 (000010).

The Kill/Inject pattern will NOT be affected. The Current and Requested BCO Counters are NOT affected.

Pulsing Data Reset will do the following:

1. Reset the Current BCO Counter to 0.

2. Reset the Requested BCO Counter to –4 (111100)

3. Reset all hit Pixels by forcing all End-of-column Command Sets to the Reset Command

4. Reset all End-of-column Priority Encoders to point to their respective Register A.

5. Reset all End-of-column Sets to “empty”.

When in Continuous Mode, TrigAcc (pad 29) must be set to Logic 0 (reject) while performing either reset. In addition, all clocks must be set to the Logic 0 state for the duration of the reset.

TrigAcc

In Continuous Mode, TrigAcc is the throttle. If the system is overloaded or if some situation arises during which it would be better NOT to accept any hits (such as resetting), TrigAcc should be set to Logic 0 (reject). This will prevent the command interpreter in each pixel from accepting hits from the analog section of each pixel. In other words, all hits will be ignored for the duration of the reject. Under normal operation, TrigAcc should be set to Logic 1 (accept).

In External Trigger Mode, TrigAcc is the Trigger signal. At the rising edge of this signal, a new external trigger scanned in along the Trigger path will be presented to the End-of-column Logic cells as the requested BCO number. The act of scanning a new trigger into the chip will not affect the requested BCO number being presented to the End-of-column Logic cells until the falling edge of the TrigAcc signal. Therefore, it is possible to scan in a new trigger while the chip is outputting data from an old trigger. The old trigger will not be corrupted as the new trigger is scanned. The new trigger will replace the old when the TrigAcc signal is pulsed.