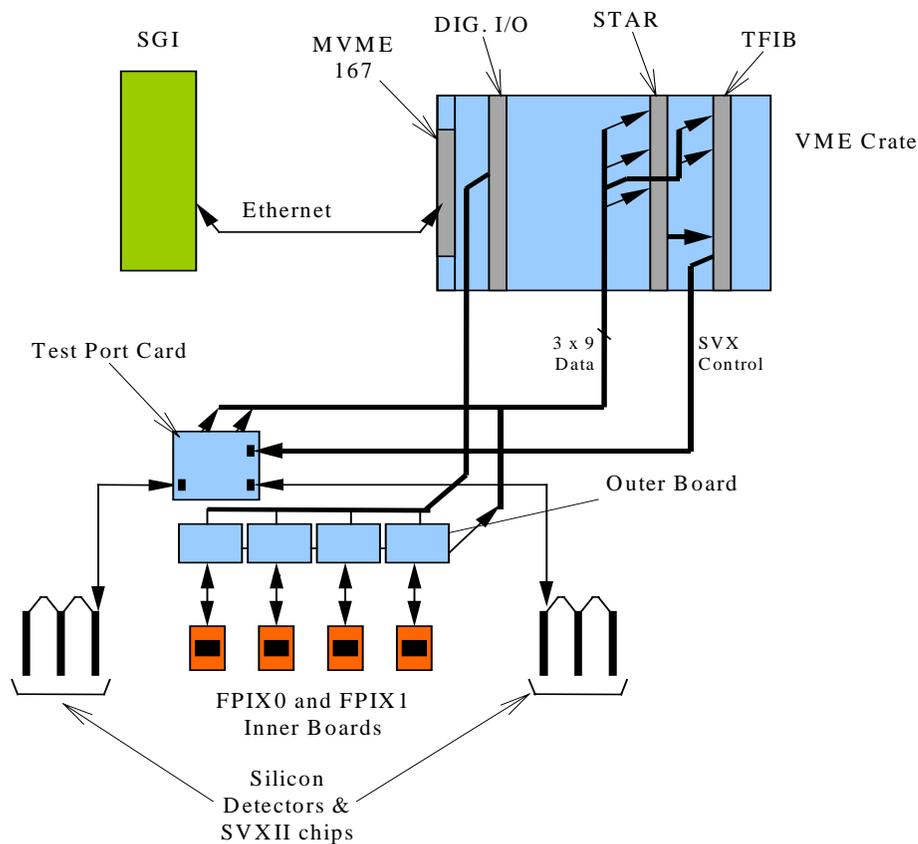# BTeV Beam Test 99

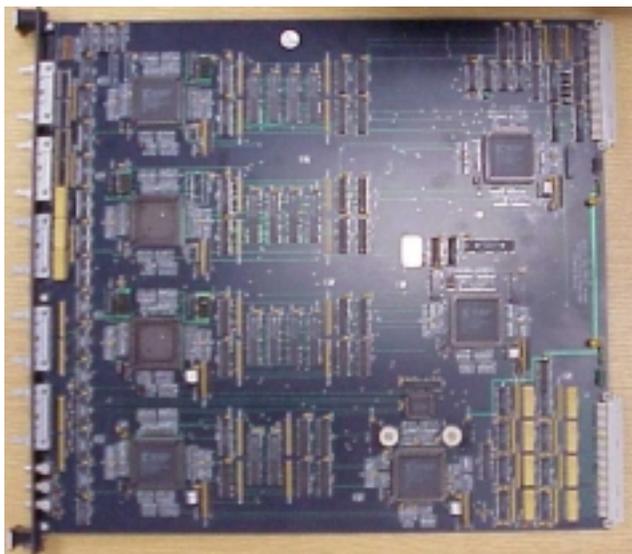## Description of the hardware

BTeV Beam Test 99

- **DAQ Hardware:**
  - STAR
  - TFIB
  - MVME
  - I/O board
  - SVX2
    - PORT CARD
    - Inner board
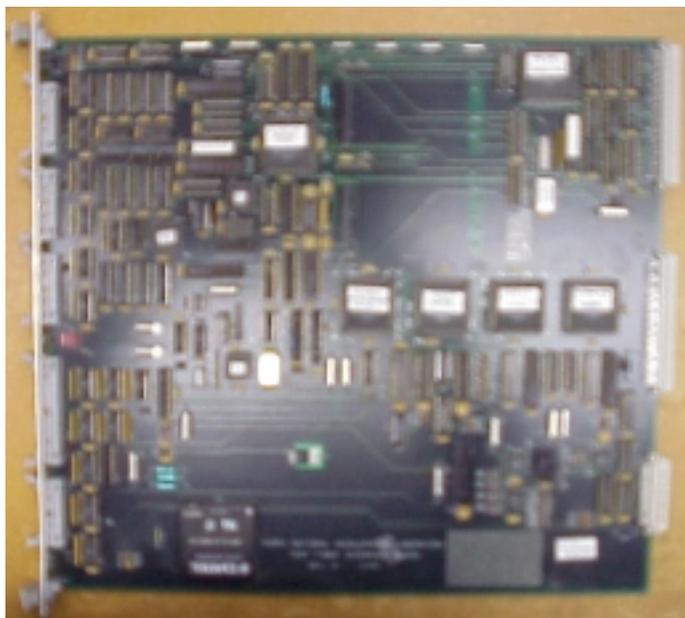 - Pixel
    - Outer board
   - Inner board

BTeV Beam Test 99 - STAR

- Generation of upper level command sequences to operate TFIB, PORT CARD and SVXII inner board;
- Three 64k byte deep data buffer;
- Data readout - 16/16 bit VME;
- 9U x 400mm VME card format;
- Interface to external cosmic rays/ scintillator triggers;
- Emulation of Tevatron beam structures.

BTeV Beam Test 99 - TFIB

- Clock provided by STAR through J3 backplane;
- Controls one PORT CARD, readout three HDIs connected to the TPC @ 26.5MBytes/s;
- Supplies SVX2 with the Calibration, Ramp-Reference and Ramp-Pedestal analog voltages;
- Differential PECL interface to TPC;
- Generates trigger to Pixel readout;
- NECESSARY ONLY FOR SVX2

BTeV Beam Test 99 - MVME
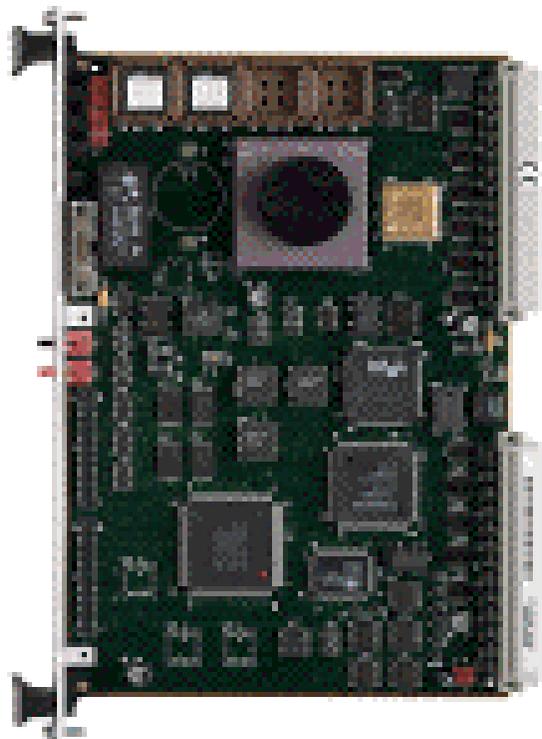
- Based on the MC68040 microprocessor;

- Achieve 26 MIPS at 25 MHz and 40 MIPS at 33 MHz;

- A16/A24/A32/D8/D16/D32/D64 VMEbus master/slave interface;

- 128KB of static RAM;

- SCSI bus interface with DMA

- Ethernet transceiver interface;

- Four serial ports with EIA-232-D interface

BTeV Beam Test 99 - I/O BOARD

Industry pack module

- Green Spring VIPC610;
- 6U VMEbus Specification;
- Conforms to the IndustryPack Logic Interface Specification;
- IndustryPack I/O mapped into the VMEbus A16/D16 space;
- 4 slots, each one interfaced with a 50-pin flat cable;
- 2 RS485 interfaces;
  - Initialization of Pixel boards
- 1 GPIB interface
  - Control of equipment
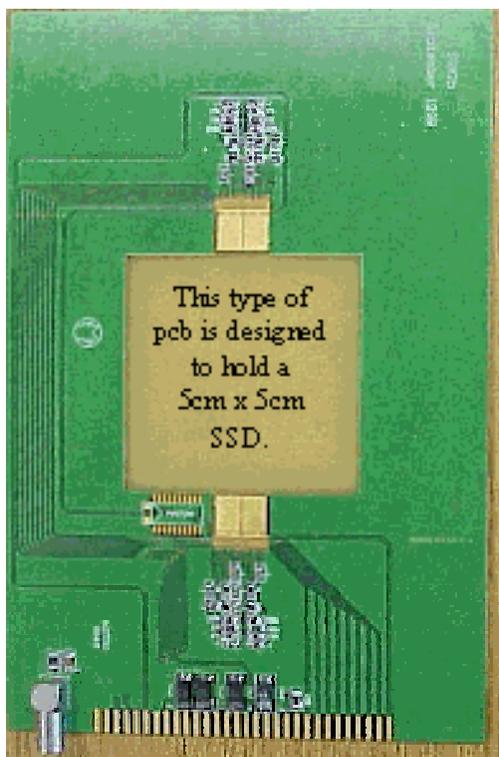
BTeV Beam Test 99 - SVX2

PORT CARD

- Three ports of initialization, control and data readout for SVX II chips;
- Executes control commands transmitted by the TFIB;
- Buffers SVX2 clock and drives the SVX2 chips;
- Recognizes the EOR word from SVX2;
- Transmits SVX2 data to STAR (Differential PECL);
- Analog control of SVX2 using DACs

BTeV Beam Test 99 - SVX2

INNER BOARD

This type of pcb is designed to hold a 5cm x 5cm SSD.

- Mechanical support for 4 SVX2 chips (128 channels readout chip) and strip detector;
- Bypass capacitors to SVX2 power supplies;
- 50-pin flat cable interface with PORT CARD;
- Resistors to calibration

BTeV Beam Test 99 - Pixel

OUTER BOARD

- On board programmable FPGA Altera 7192
- Interfaces available:
  - RS485 - Initialization;
  - PECL - Readout to STAR;
  - ECL - Daisy chain of several outer boards;
  - NIM - Trigger inputs;
  - Low Voltage Single Ended(0~3.3V) to control and readout the Pixel chip;
- Responsible for building the events to STAR from Pixel raw data;
- Same outer board for FPIX1 and FPIX0, just a different firmware

BTeV Beam Test 99 - Pixel

FPIX0 INNER BOARD
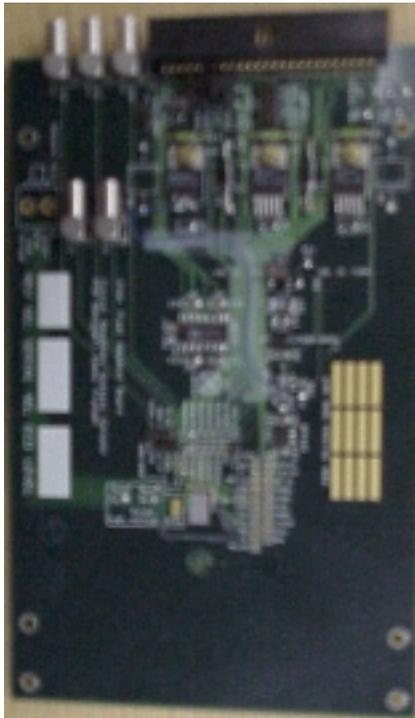
- Mechanical support for FPIX0 (64 x 12 pixel readout chip) and detector
- Voltage regulators for voltage power supplies of FPIX0;
- Bypass capacitors for voltage supplies;
- Analog output of FPIX0 goes to:
  - 1:1 buffer;
  - Operational Amplifier - gain and offset;
  - 8 bit ADC;
- 50-pin connector that delivers raw data to outer board;

BTeV Beam Test 99 - Pixel

FPIX1 INNER BOARD

- Mechanical support for FPIX1 (160 x 18 pixel readout chip) and detector
- Bypass capacitors for voltage power supplies;
- Daughter board:
  - Mounted in the top of the inner board makes the pin out compatible with outer board;
  - 50-pin connector delivers raw data to outer board;