

Pixels for CDFII in Run IIb

Precision tracking in the high radiation collider environment for a Higgs discovery at the Tevatron before LHC turn-on.

- **Replace Layer00 strips with pixels**
 - radiation survivability to 30 Mrad / 30 fb⁻¹ is desirable
 - pattern recognition: 3.3 M channels vs 14 K channels
 - z resolution 60-120 μm possible
 - large S:N helps r- ϕ resolution, trigger, etc.
- **Pixels are feasible for ~2004**
 - ATLAS-style sensors in production
 - FPIX readout chip in advanced prototype
 - cost and schedule fits into RunIIb plans
- **Overlap with BTeV and D0**
 - BTeV 10% scale test is comparable
 - Economy of scale (preproduction/production quantities)
 - Initial sharing of resources (personnel and financial)

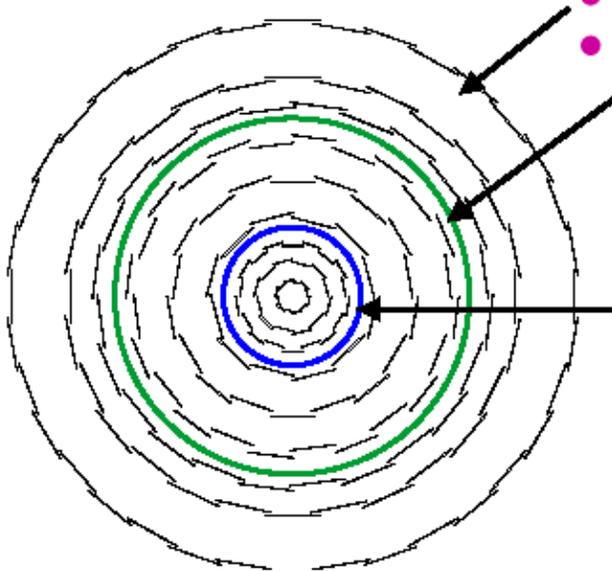
Pixels are the preferred technology and they are available to CDF. CDF needs to decide soon (Jan. 2001) whether to pursue this option for RunIIb.

RunIIb Replacement Silicon

- SVXII designed for 2 fb-1
- Laboratory has initial guidelines
 - 15 fb-1 by 2007
 - Minimal upgrade (\$2.5M)
 - Minimal shutdown (~ 6 months)
- Nov PAC: CDF to respond to
 - Layer00 only replacement
 - Partial replacement
 - Full replacement
- RunIIb replacement silicon WG
 - Evaluated longevity expectations
 - Evaluated effort and critical items for various options

CDF silicon system

- L00, L0, L1, L2, (L4) at risk
 - $S/N < 6$ or can't fully deplete
 - Huge uncertainties: 3-12 fb⁻¹
- Partial replacement not viable
- “SVX4” chip development is the critical item to start
- Pixel option



- Goal: Keep or improve functionality
- Retain ISL (~ 8 krad/fb⁻¹)
- 2 New Radial Groups

> Outer

- Design to last a long time
- Simple:
 - two single-sided sensor designs
 - one double-sided hybrid design
 - carbon fiber supports with cooling

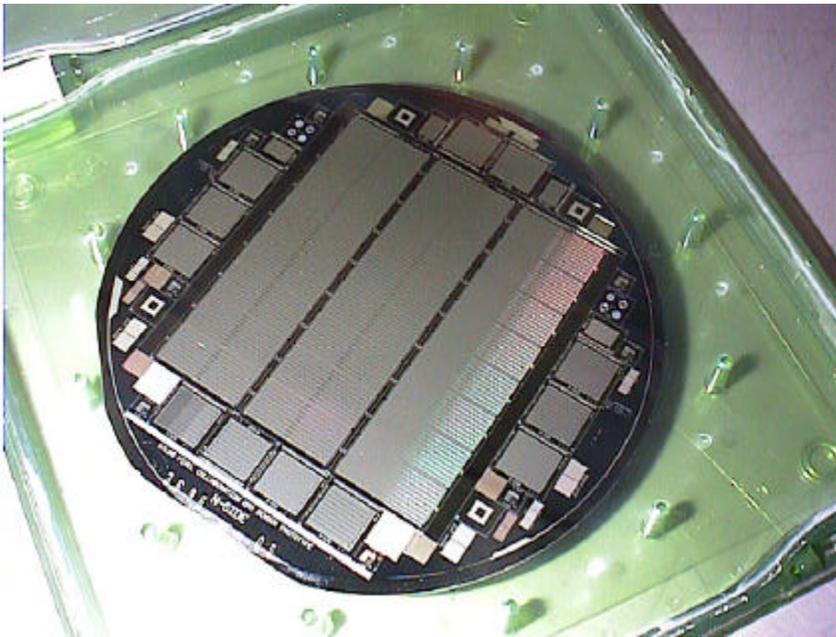
> Inner (within blue circle)

- Design to last minimum of 15 fb⁻¹
- Integrated cooling at lower temp.
- Two outermost layers w/simple design:
 - 2 single sided sensor designs
 - L00 style hybrid design
- Innermost layer: L00 replacement
 - Exact replacement
 - Could use pixels if ready and sufficiently lightweight.

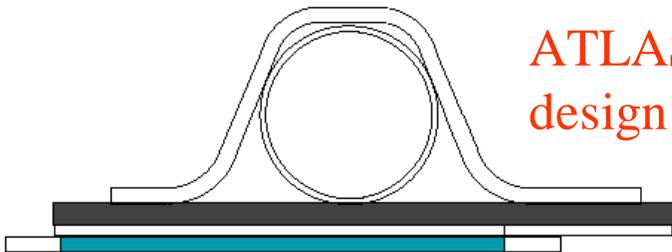
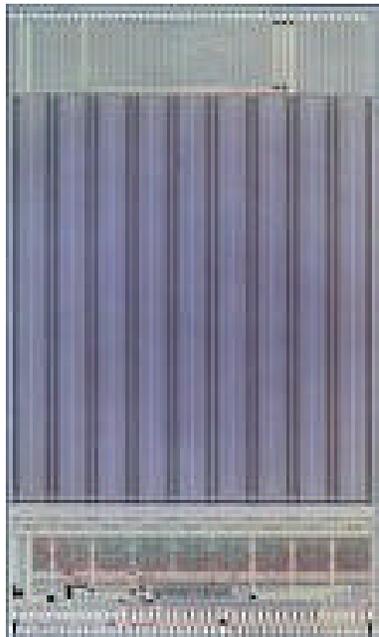
Full replacement concept

Pixel concept

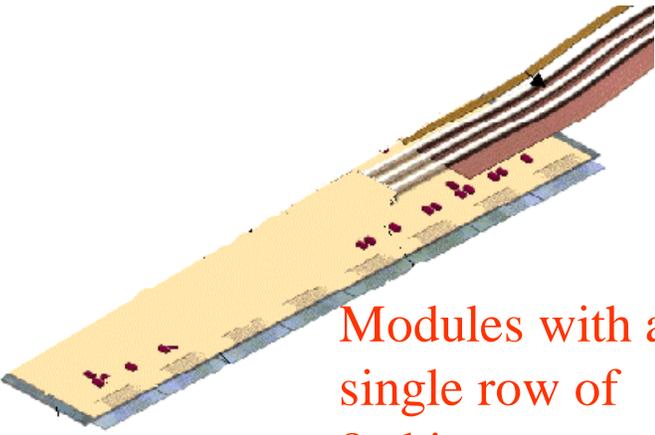
ATLAS WAFER



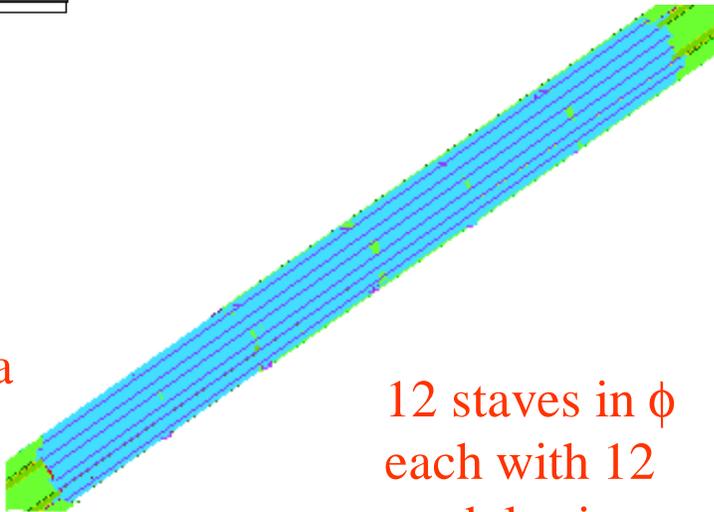
FPIX1 chip



ATLAS stave design



Modules with a single row of 8 chips



12 staves in ϕ each with 12 modules in r-z

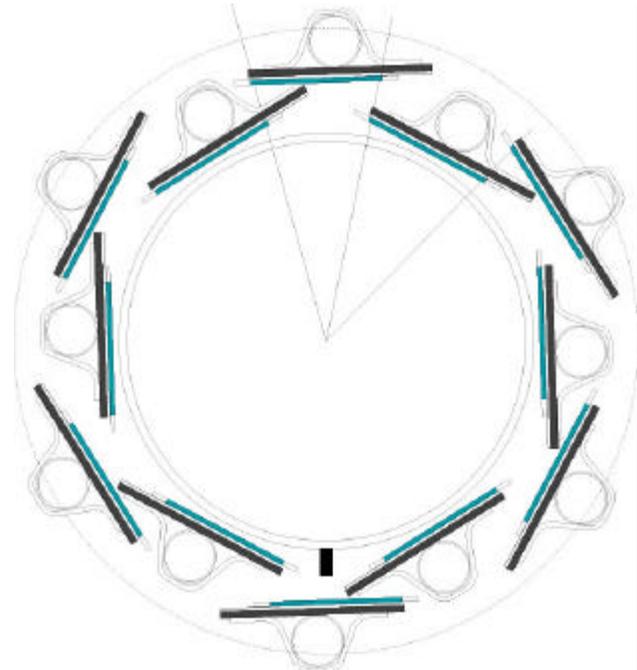
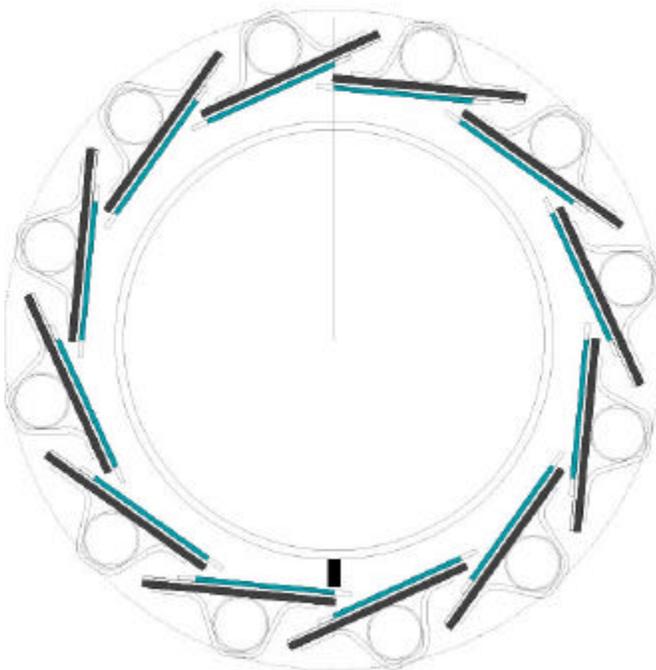
Pixel concept

Channel Count

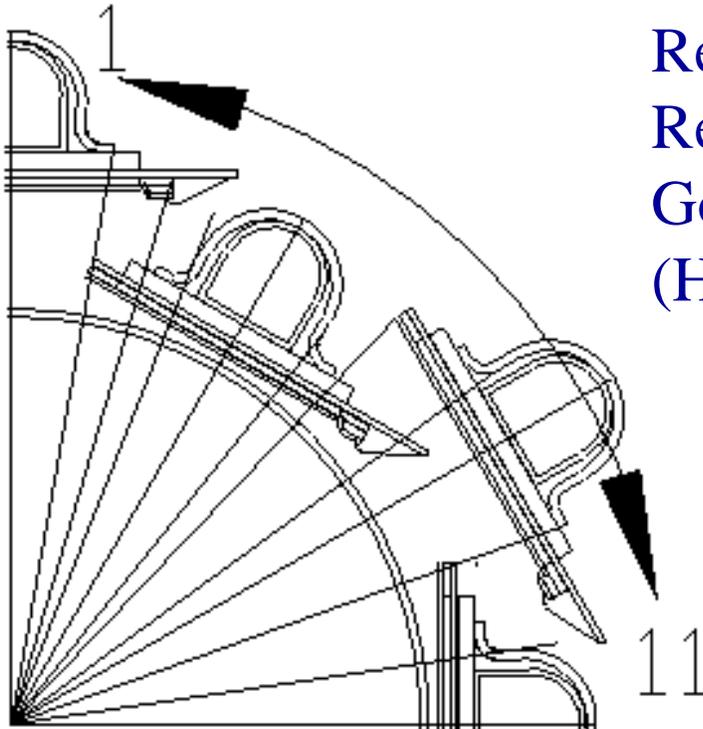
| | | |
|------------------------------------|--------------------------------------|---------------------|
| Pixel cell | 50 μm x 400 μm | 1 channel |
| Pixel cell (between readout chips) | 50 μm x 600 μm | 1 channel |
| FPIX chip | 18 columns x 160 rows | 2,880 channels |
| Sensor/Module | single row of 8 FPIX chips | 23,040 channels |
| Ring | 12 modules in ϕ | 276,480 channels |
| Complete detector | 12 rings along z | 3, 317,760 channels |

Mechanical

| | | |
|-----------|--|-------------------|
| FPIX chip | total area (assumes 3mm for periphery and bonding pads+100 μm all around) | 0.82 cm x 0.77 cm |
| FPIX chip | thickness | 280 μm |
| Sensor | active area | 0.8 cm x 5.90 cm |
| Sensor | total area (assumes 1mm guard ring) | 1 cm x 6.10 cm |
| Sensor | thickness | 280 μm |
| Sensor | inner layer innermost radius (closest surface to beam pipe) | 1.33 cm |
| Sensor | outer layer innermost radius | 1.60 cm |
| Detector | length in z (assumes 1.5mm between modules) | 75cm |



Material estimate



Regions of 4 layers of Si
 Regions of cooling
 Goal is $< 2.5\% X_0$
 (HDI adds $0.1\% X_0$)

| Region | % | Si | kapton | Cu | C fiber | Al | H ₂ O/Glycol | Alumina | X/X ₀ (%) | Tot. |
|---------------------|------|------|--------|------|---------|-----|-------------------------|---------|----------------------|------|
| X ₀ (mm) | | 93.6 | 284 | 14.3 | 220 | 89 | 361 | 72 | | |
| 1 | 11.2 | 450 | 200 | 3 | 1000 | 400 | 2000 | 0 | 2.03 | 0.23 |
| 2 | 7.0 | 900 | 400 | 46 | 400 | 0 | 0 | 120 | 1.77 | 0.12 |
| 3 | 5.6 | 650 | 200 | 43 | 700 | 0 | 0 | 0 | 1.38 | 0.08 |
| 4 | 9.6 | 450 | 200 | 3 | 1000 | 400 | 2000 | 0 | 2.03 | 0.19 |
| 5 | 9.2 | 450 | 200 | 3 | 1000 | 400 | 2000 | 0 | 2.03 | 0.19 |
| 6 | 6.1 | 450 | 200 | 3 | 700 | 0 | 0 | 0 | 0.89 | 0.05 |
| 7 | 10.1 | 900 | 400 | 46 | 400 | 0 | 0 | 120 | 1.77 | 0.18 |
| 8 | 7.9 | 450 | 200 | 3 | 1000 | 400 | 2000 | 0 | 2.03 | 0.16 |
| 9 | 11.3 | 450 | 200 | 3 | 1000 | 400 | 2000 | 0 | 2.03 | 0.23 |
| 10 | 12.6 | 900 | 400 | 46 | 700 | 0 | 0 | 120 | 1.91 | 0.24 |
| 11 | 9.4 | 450 | 200 | 3 | 1000 | 400 | 2000 | 0 | 2.03 | 0.19 |
| Total | | | | | | | | | | 1.87 |

Pixel DAQ concept

- Hits stored in cell
- Readout via column logic
- FPIX sends data to a pixel port card (serialized?)
- optical link to a pixel-FIB
- FIB controls pixels and receives data in a deep memory module, time orders hits, matches to L1 accept, sends data to VRB.
- Concept exists that pixel-FIB combines hits into “strips” for SVT trigger

Cost

Overlaps with BTeV 10% scale test

| Description | Quantity | | | Unit (\$K) | Units | Cost (\$K) | Cost w/ contingency |
|------------------|----------|-------|-------|---------------|------------|----------------|------------------------|
| | Base | Spare | Total | | | | |
| Sensors NRE | 0.5 | | 0.5 | 25 | each | 12.5 | 16.3 |
| Sensors | 24 | 26 | 50 | 1 | wafers | 50.0 | 65.0 |
| FPIX | 1152 | 1700 | 2852 | 0.03 | chips | 96.0 | 124.8 |
| Bump bonding | 24 | 14 | 38 | 2.9 | wafers | 110.2 | 165.3 |
| Module R&D | 12 | | 12 | 4 | modules | 48.0 | 72.0 |
| Modules | 144 | 84 | 228 | 0.58 | modules | 132.2 | 198.4 |
| HDI cables | 144 | 84 | 228 | 0.50 | cable sets | 114.0 | 171.0 |
| Pixel port card | 24 | 6 | 30 | 3 | boards | 90.0 | 135.0 |
| High voltage | 24 | | 24 | 3 | supplies | 72.0 | 108.0 |
| Low voltage | 24 | | 24 | 2 | supplies | 48.0 | 72.0 |
| Monitoring | 1 | | 1 | 20 | system | 20.0 | 30.0 |
| Interlocks | 1 | | 1 | 20 | system | 20.0 | 30.0 |
| Pixel-Fib | 24 | 6 | 30 | 5 | boards | 150.0 | 195.0 |
| Opto-electronics | 1152 | 348 | 1500 | 0.03 | each | 45.0 | 67.5 |
| DAQ cables | 24 | 6 | 30 | 1 | bundles | 30.0 | 45.0 |
| Staves R&D | 2 | | 2 | 20 | each | 40.0 | 60.0 |
| Staves | 12 | 3 | 15 | 3 | each | 45.0 | 67.5 |
| Stave support | 1 | | 1 | 20 | system | 20.0 | 30.0 |
| Cooling manifold | 1 | | 1 | 20 | system | 20.0 | 30.0 |
| Cooling system | 1 | | 1 | 20 | system | 20.0 | 30.0 |
| Total | | | | | | \$1,178 | \$1,705 |

Round numbers: \$2.0M for CDF alone

\$1.5M for CDF/BTeV

\$1.0M for CDF/BTeV/D0

Schedule

FY01: FPIX and module R&D done by BTeV

Mechanical design: two 0.5 FTE engineers:
system mock-up and carbon prototypes

DAQ design: CDF pixel test stand

Specify pixel port card/pixel-FIB

2002: Order sensors and readout chips

Mechanical and DAQ prototypes

Begin module assembly

2003: Finish module assembly and test

Build and assemble staves

DAQ production

Oct 2003: Ready for data

Initial CDF groups: FNAL, UC Davis, CMU,
New Mexico, Rutgers, LBNL, Purdue, +others
(new institutions, new assistant professors).

*Hope is that the joint project will benefit both
the current collider experiments and BTeV*

CDF pixels

<http://www-rhvd.fnal.gov/wester/>

Pixel Concept for CDFII

A pixel detector at the innermost radius for precision vertexing at high luminosity

This page is under construction and some links may be password protected. This page is intended for internal communication between those interested in exploring a pixel option for CDFII in Run IIb. Much of this information is potentially useful for D0 consideration of an inner pixel system as well.

Overview

We consider the advantages and feasibility of replacing an irradiated Layer00 silicon strip detector by a pixel system for Run IIb running and beyond. The possible advantages include increased radiation survivability up to 30 fb⁻¹ or more, improved impact parameter resolution, large S/N with very high efficiency, and improved pattern recognition for associating hits to tracks. The feasibility of installing this system relies on the advanced R&D of similar systems. In particular, the FPIX series of readout chips bump bonded to ATLAS style sensors has already achieved excellent performance in beam tests. The DAQ for the pixel system is expected to have many similarities to a system under development for the proposed BTeV experiment. We recognize that this system is conceptually new for CDFII and we recommend that a Layer00 strip replacement also be pursued simultaneously until clear advantages of a pixel system and minimal risk for project completion can be demonstrated.

Key Points

| | |
|--------------------------------|--|
| Radiation survivability | Pixels increase that probability that only one replacement need to be performed |
| Feasibility | Estimate is that both production sensors and chips could be ordered by the end of 2001 |
| FNAL expertise | Rad hard vertex, ASIC design, and ESE groups have worked for several years on pixels |
| CDF expertise | Strong involvement in both ATLAS and CMS pixels as well as diamond R&D |
| Tracking performance | Excellent position resolution and pattern recognition capabilities |
| Physics performance | To be quantified is the impact on <i>b</i> -tagging needed for Higgs search |
| Cost | Minimal due to the overlap with the current BTeV R&D efforts |

Specifications at a glance

| | |
|--|---|
| Geometry option 1 - staggered option | Geometry option 2 - tilted option |
| Specifications for option 1 | |

Sub topics

| | |
|--|--|
| Radiation resistance | Tracking performance |
| FPIX readout chip | DAQ components |
| Sensors | Power supplies |
| Modules and bump bonding | Mechanical including material budget |
| Low mass HDI cable | Cooling |
| Pixel port card | Physics capabilities |

Documents

First CDFII Replacement Silicon Workshop Mar 15, 2000: [agenda](#), [pixel talk \(pdf\)](#)
Second CDFII Replacement Silicon Workshop June 14, 2000: [agenda](#), [pixel talks](#)
Third CDFII Replacement Silicon Workshop July 11, 2000: [agenda](#), [pixel talks](#)
Fourth CDFII Replacement Silicon Workshop Aug 8, 2000: [agenda](#), [pixel talks](#)
Special Pixel subgroup meeting Sept 20, 2000: [agenda](#), [pixel talks](#)

Draft proposal for initial report to CDF review committee: [pdf](#), [ps](#)
Proposal for the October report to CDF review committee: [pdf](#), [ps](#)
Current version of the draft (in progress): [history](#), [pdf](#), [ps](#), [LaTeX](#) and [figures](#)

Links

[UC Davis CDF pixel page](#)
[CDF RunIIb web page \(CDF internal page\)](#)
[D0 pixel page](#)
[FNAL radiation hard vertex group](#)
[ATLAS pixel system overview](#)
[CMS pixel system overview](#)

D0 pixels

Ela Barberis
Meenakshi Narain
Gordon Watts

<http://d0.phys.washington.edu/Projects/Pixels/>

Run 2b Pixels

The Detector and Environment

- ✗ [Detector Specification](#) (size, geometry, etc.)
 - ✗ [Pixel Detector Properties](#)
 - ✗ [Cabling](#)
 - ✗ [Cooling](#)
- ✗ Resolution & Occupancy Calculations
- ✗ Readout
 - ✗ [Triggering](#)
 - ✗ Pixel Readout Issues
- ✗ [Schedule & Cost](#)

Group Activities & References

- ✗ [Run2b Review Panel](#)
- ✗ Talks Given
 - ✗ [Pixel Update](#) - 9/15/00 Run2b Meeting
 - ✗ [Pixel Readout Development & Status](#) -- 9/1/00 Run 2b Meeting
 - ✗ [Inner Pixels](#) -- General Proposal 6/21/00 Run 2b Meeting
 - ✗ [Pixels](#) -- General Intro Talk given by W. Wester 4/14/00 Run 2b Meeting
- ✗ Documents
 - ✗ [Full BTeV PAC Proposal](#) (Pixels are in chapter 4, starting on page 61)
 - ✗ [ATLAS Pixel TDR](#)
 - ✗ [Inner Tracker and L1 Trigger Based on Pixel Detectors for D033](#) (D0 Note 3409)
 - ✗ [Very initial version of CDF Pixel expression of intent](#)
- ✗ Other Home Pages
 - ✗ [CDF Run2b Pixel Home Page](#)
 - ✗ [Fermilab Pixel Group Home Page](#)
 - ✗ [D0 Run 2 Silicon Home Page](#)
 - ✗ [ATLAS Pixel Home Page](#)

