

Pixels for CDFII in Run IIb

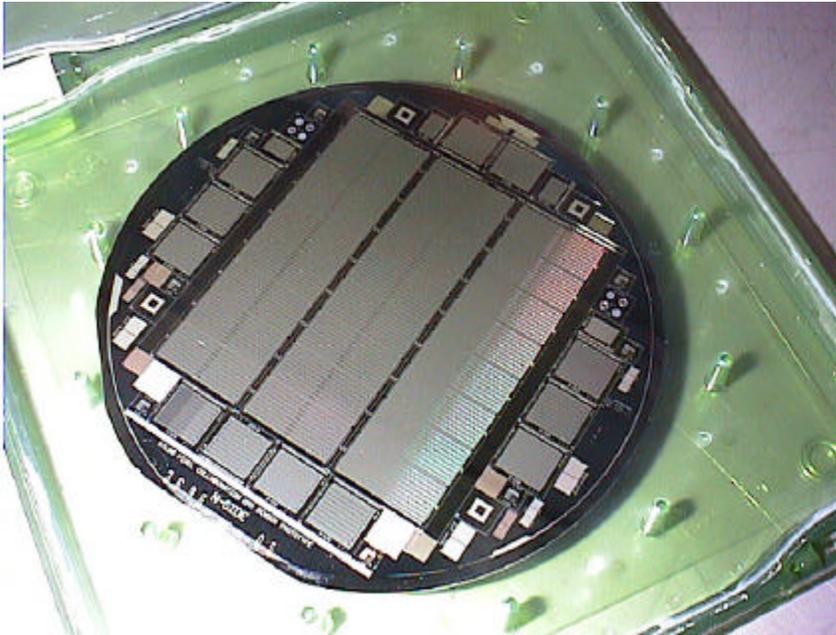
Precision tracking in the high radiation collider environment for a Higgs discovery at the Tevatron before LHC turn-on.

- **Replace Layer00 strips with pixels**
 - radiation survivability to 30 Mrad / 30 fb⁻¹ is desirable
 - pattern recognition: 3.3 M channels vs 14 K channels
 - z resolution 60-120 μm possible
 - large S:N helps $r\text{-}\phi$ resolution, trigger, etc.
 - keep Layer00 strip option a fallback
- **Pixels can be ready for 2004**
 - ATLAS-style sensors in production
 - FPIX readout chip in advanced prototype
 - cost and schedule fits into RunIIb plans
- **Overlap with BTeV and D0**
 - BTeV 10% scale test is comparable
 - Economy of scale (preproduction/production quantities)
 - Initial sharing of resources (personnel and financial)

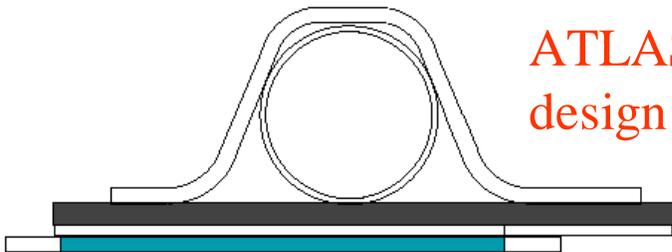
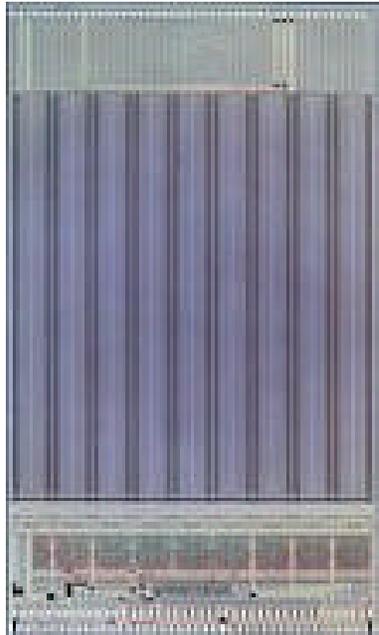
Pixels are the preferred technology and they are available to CDF. CDF needs to decide soon (Jan. 2001) whether to pursue this option for RunIIb.

Pixel concept

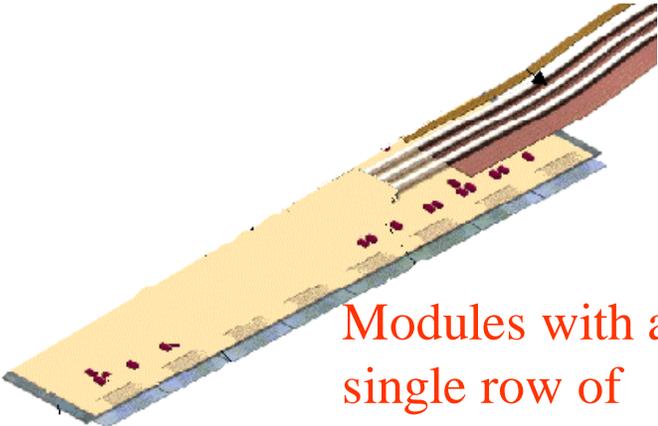
ATLAS WAFER



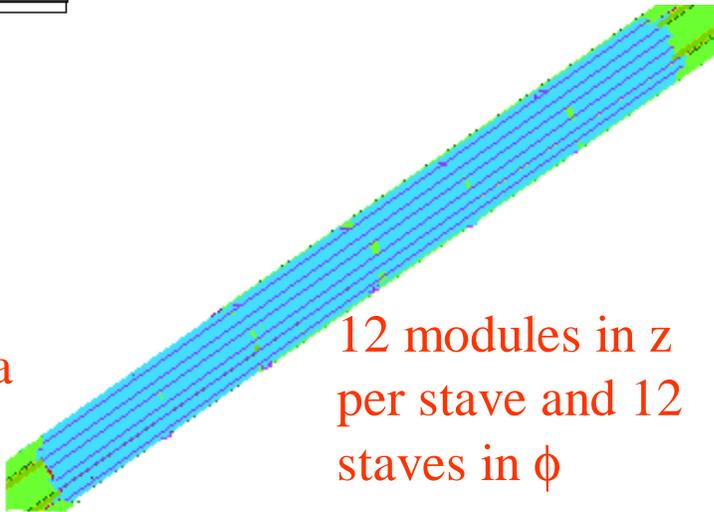
FPIX1 chip



ATLAS stave design



Modules with a single row of 8 chips



12 modules in z per stave and 12 staves in ϕ

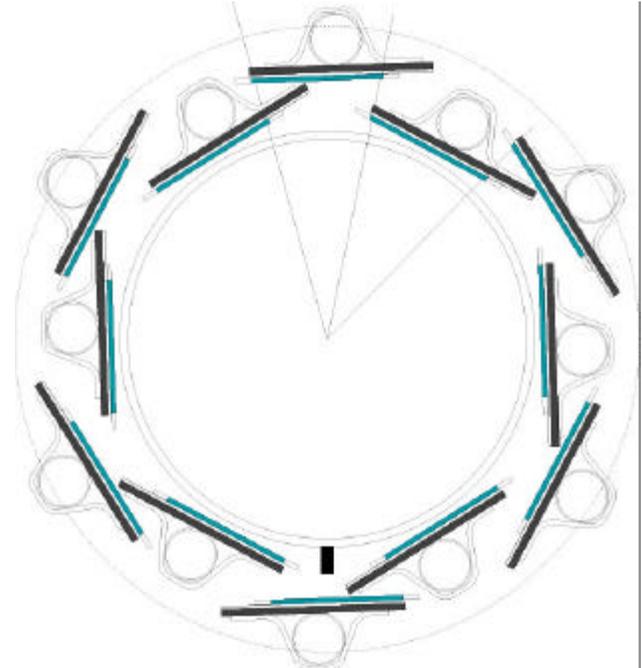
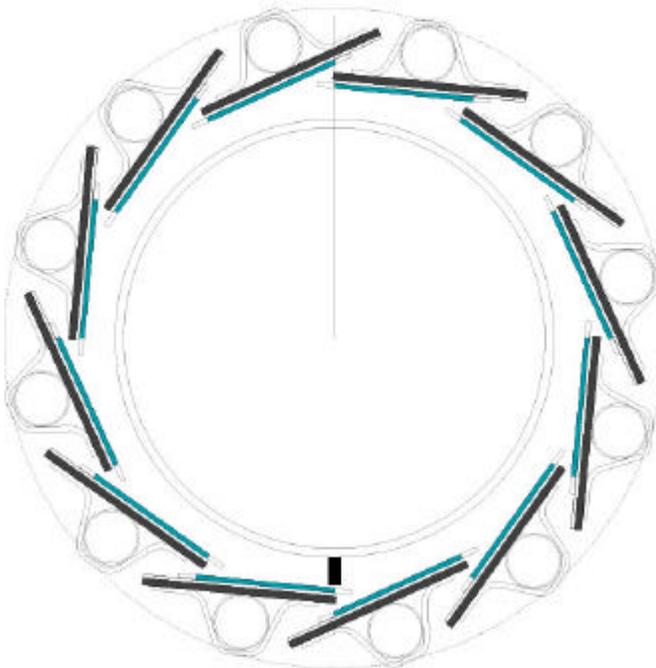
Pixel concept

Channel Count

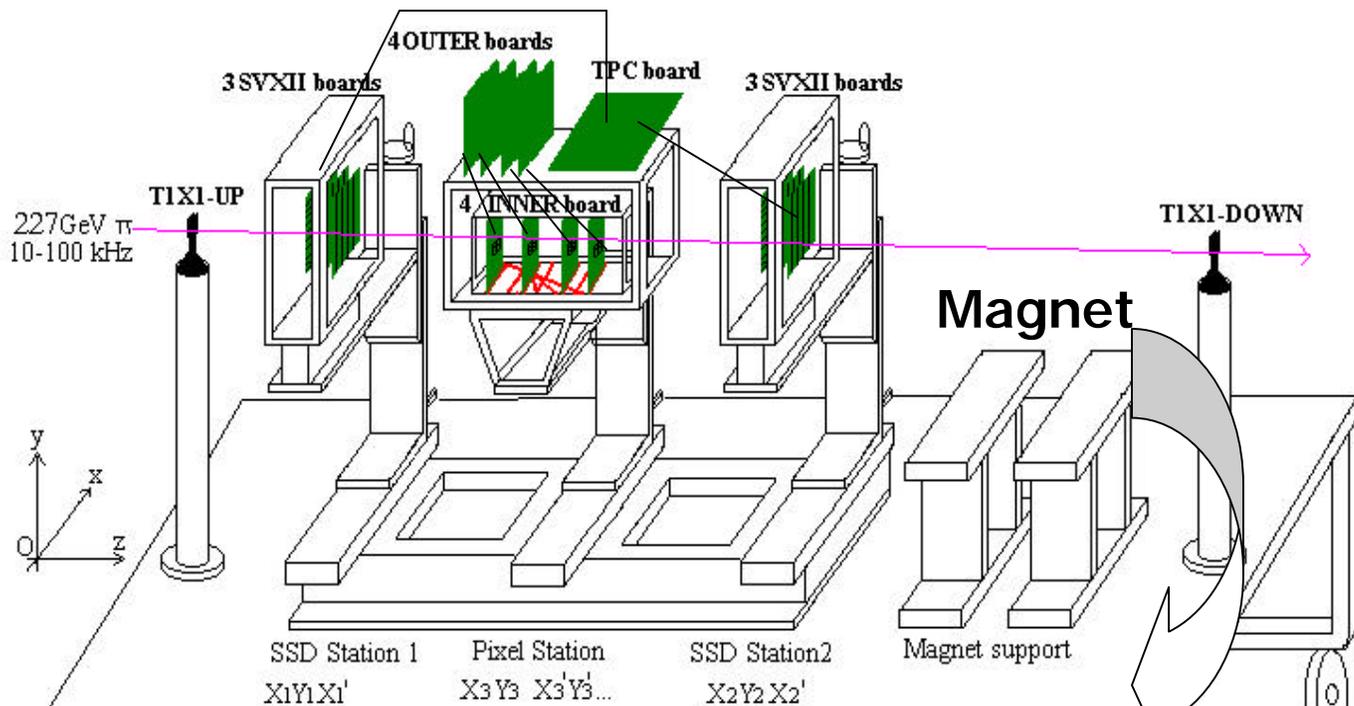
Pixel cell	$50\ \mu\text{m} \times 400\ \mu\text{m}$	1 channel
Pixel cell (between readout chips)	$50\ \mu\text{m} \times 600\ \mu\text{m}$	1 channel
FPIX chip	18 columns x 160 rows	2,880 channels
Sensor/Module	single row of 8 FPIX chips	23,040 channels
Stave	12 modules along z	276,480 channels
Complete detector	12 staves in ϕ	3, 317,760 channels

Mechanical

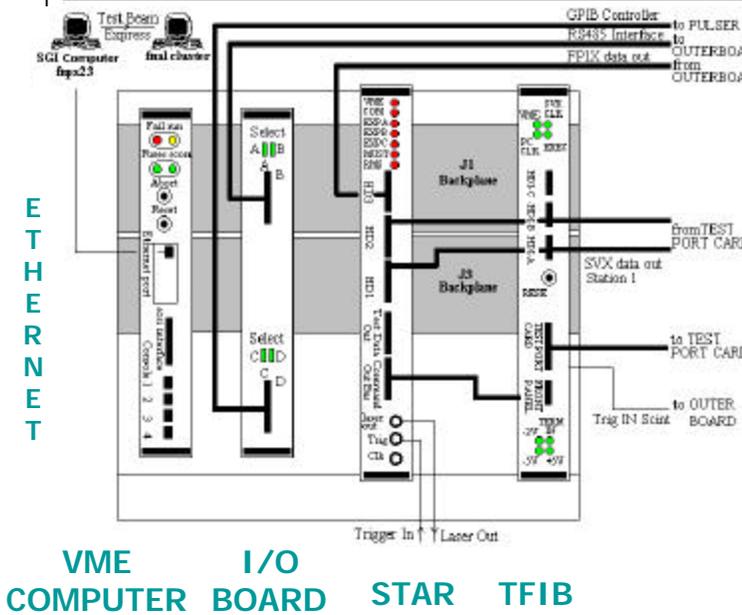
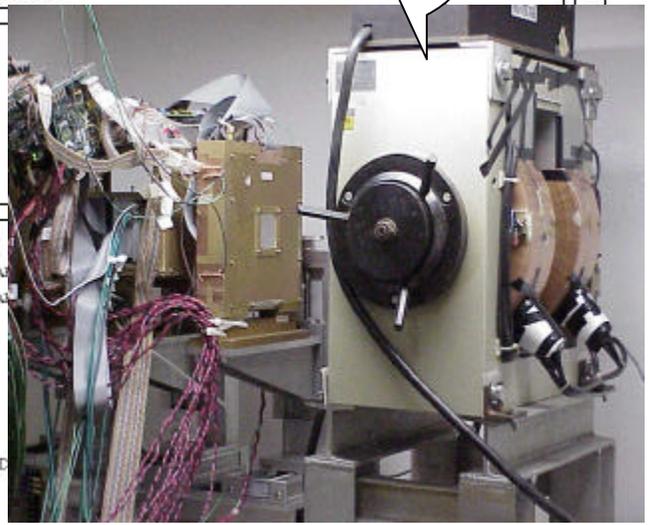
FPIX chip	total area (assumes 3mm for periphery and bonding pads+100 μm all around)	0.82 cm x 0.77 cm
FPIX chip	thickness	200 μm
Sensor	active area	0.8 cm x 5.90 cm
Sensor	total area (assumes 1mm guard ring)	1 cm x 6.10 cm
Sensor	thickness	250 μm
Sensor	inner layer innermost radius (closest surface to beam pipe)	1.33 cm
Sensor	outer layer innermost radius	1.60 cm
Detector	length in z (assumes 1.5mm between modules)	75cm



Pixel Testbeam (courtesy of G. Chiodini)



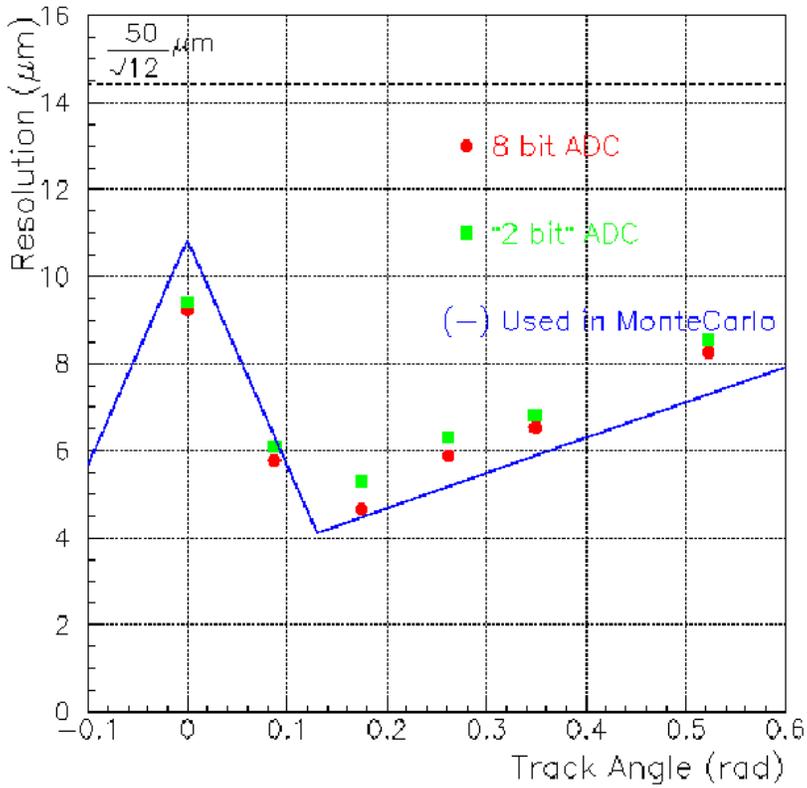
DAQ



- I/O Board
 - Controls and Initializes 4 Pixel readout chips
 - GPIB controller: HV, thresholds, and pulser
- Automatic pixel calibration

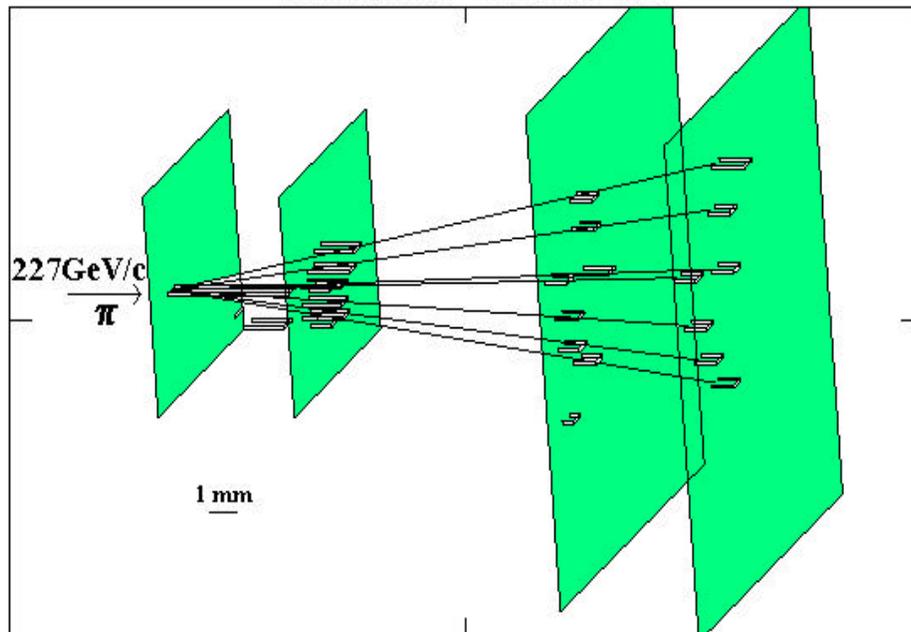
Testbeam results

Pixel Resolution (FPIX0)

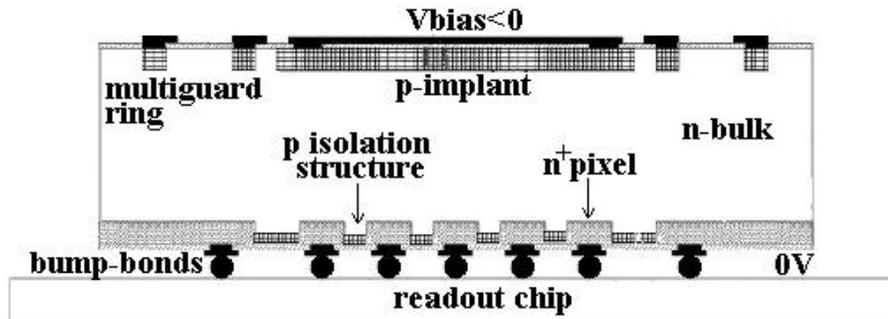


Position resolution better than $8 \mu\text{m}$ for most track angles

Run: 7358 Event: 478



ATLAS Sensors



- Radiation hard to 10^{15} n/cm²
- ATLAS devices in production
- CiS and Tesla are chosen vendors
- Univ of New Mexico
 - Leads ATLAS sensor development
 - Testing capabilities + procedures established
- Sensors can be ordered FY02
 - GDS file requires modifications
 - Some care for bricking geometry
 - Place order (overlap with BTeV)
 - \$60-100K = 300 sensors (need 144)

FPIX chip

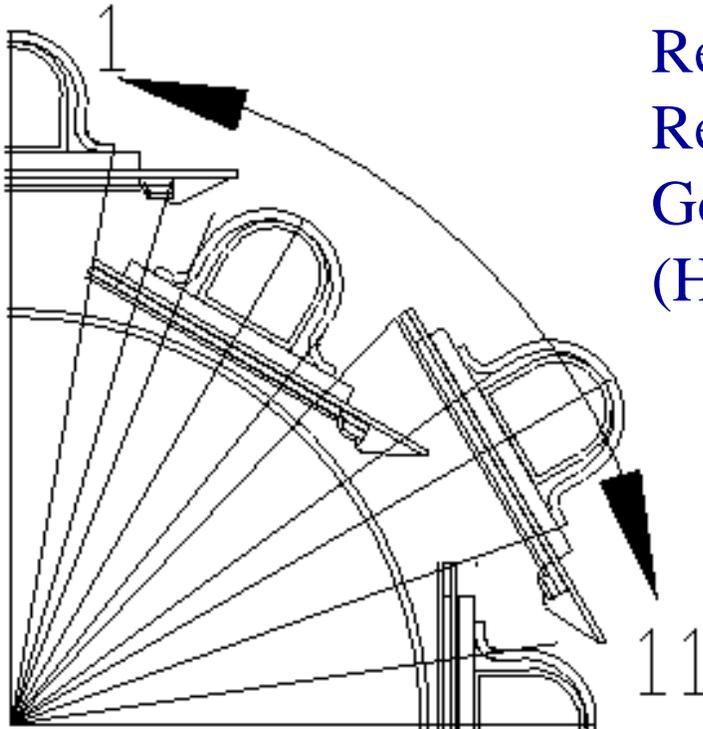
- CDF can use the BTeV chip developed by the FNAL ASIC group
- Production chip in Oct 2001 planned
 - FPIX0 (1997) HP 0.8 μm CMOS
 - 12 x 64
 - analog digitized off chip
 - Beam tests
 - FPIX1 (1998) HP 0.5 μm CMOS
 - 18 x 160
 - 2-bit FADC (new R/O architecture)
 - Beam tests
 - Pre-FPIX2T (1999) TSMC 0.25 μm CMOS
 - 2 x 160
 - 3-bit FADC (no EOC logic)
 - Co-60 exposure to > 30 Mrads
 - Pre-FPIX2I (2000) “CERN” 0.25 μm CMOS
 - 18 x 32
 - Complete core with simplified EOC and R/O
 - Due on Monday
 - Pre-FPIX2-T2 (2000) TSMC 0.25 μm CMOS
 - 18 x 64
 - Internal DACs, programming interface
 - Due in Dec 2000

10 wafers = 2000 good chips
\$160K for 1st 10 + \$32K for 2nd

Mechanical

- Module overlaps with BTeV
 - Bump bonding at UC Davis
 - Bump yields $\sim 1:10^4$
 - MCNC and 3 vendors in Europe qualified
 - Actual processing time small (two months)
- Stave and barrel unique to CDF
- Use ATLAS design as the concept
- FY01 R&D requests
 - Engineer 0.5 FTE: system mock-up \$10K
 - Beam pipe, cooling, cable routing, alignment
 - Engineer 0.5 FTE: stave prototypes \$20K
 - Verify stave concept and assembly
 - Cooling tests \$10K
 - Establish temperature profile vs stave position
 - Lead engineer needs to be identified
- Exact duplicate for D0?
- Need to talk with ATLAS experts

Material estimate



Regions of 4 layers of Si
 Regions of cooling
 Goal is $< 2.5\% X_0$
 (HDI adds $0.1\% X_0$)

Region	%	Si	kapton	Cu	C fiber	Al	H ₂ O/Glycol	Alumina	X/X ₀ (%)	Tot.
X ₀ (mm)		93.6	284	14.3	220	89	361	72		
1	11.2	450	200	3	1000	400	2000	0	2.03	0.23
2	7.0	900	400	46	400	0	0	120	1.77	0.12
3	5.6	650	200	43	700	0	0	0	1.38	0.08
4	9.6	450	200	3	1000	400	2000	0	2.03	0.19
5	9.2	450	200	3	1000	400	2000	0	2.03	0.19
6	6.1	450	200	3	700	0	0	0	0.89	0.05
7	10.1	900	400	46	400	0	0	120	1.77	0.18
8	7.9	450	200	3	1000	400	2000	0	2.03	0.16
9	11.3	450	200	3	1000	400	2000	0	2.03	0.23
10	12.6	900	400	46	700	0	0	120	1.91	0.24
11	9.4	450	200	3	1000	400	2000	0	2.03	0.19
Total										1.87

Pixel DAQ concept

- Hits stored in cell. Associated with BCO
- Readout via column logic. 25MHz
- FPIX sends serialized data over HDI to a pixel port card. 24 bits/hit
- optical link to a pixel-FIB.
- Pixel-FIB controls pixels and receives data in a deep memory module, time orders hits, matches to L1 accept, sends data to VRB.
- Concept that pixel-FIB combines hits into “strips” for SVT trigger. S/N, 12 fold- ϕ
- Fermilab ESE group pixel-FIB “quite straight forward.”
- FY01 R&D requests.
 - \$10K pixel test stand
 - Specify pixel-FIB and pixel port card
 - Large overlap with BTeV’s FY01 plans

Cost

Overlaps with BTeV 10% scale test

Description	Quantity			Unit (\$K)	Units	Cost (\$K)	Cost w/ contingency
	Base	Spare	Total				
Sensors NRE	0.5		0.5	25	each	12.5	16.3
Sensors	24	26	50	1	wafers	50.0	65.0
FPIX	1152	1700	2852	0.03	chips	96.0	124.8
Bump bonding	24	14	38	2.9	wafers	110.2	165.3
Module R&D	12		12	4	modules	48.0	72.0
Modules	144	84	228	0.58	modules	132.2	198.4
HDI cables	144	84	228	0.50	cable sets	114.0	171.0
Pixel port card	24	6	30	3	boards	90.0	135.0
High voltage	24		24	3	supplies	72.0	108.0
Low voltage	24		24	2	supplies	48.0	72.0
Monitoring	1		1	20	system	20.0	30.0
Interlocks	1		1	20	system	20.0	30.0
Pixel-Fib	24	6	30	5	boards	150.0	195.0
Opto-electronics	1152	348	1500	0.03	each	45.0	67.5
DAQ cables	24	6	30	1	bundles	30.0	45.0
Staves R&D	2		2	20	each	40.0	60.0
Staves	12	3	15	3	each	45.0	67.5
Stave support	1		1	20	system	20.0	30.0
Cooling manifold	1		1	20	system	20.0	30.0
Cooling system	1		1	20	system	20.0	30.0
Total						\$1,178	\$1,705

Round numbers: \$2.0M for CDF alone

\$1.5M for CDF/BTeV

\$1.0M for CDF/BTeV/D0

\$0.5M easily swapped onto BTeV or CDF.

Schedule

FY01: FPIX and module R&D done by BTeV

Mechanical design: two 0.5 FTE engineers:
system mock-up and carbon prototypes

DAQ design: CDF pixel test stand

Specify pixel port card/pixel-FIB

2002: Order sensors and readout chips

Mechanical and DAQ prototypes

Begin module assembly

2003: Finish module assembly and test

Build and assemble staves

DAQ production

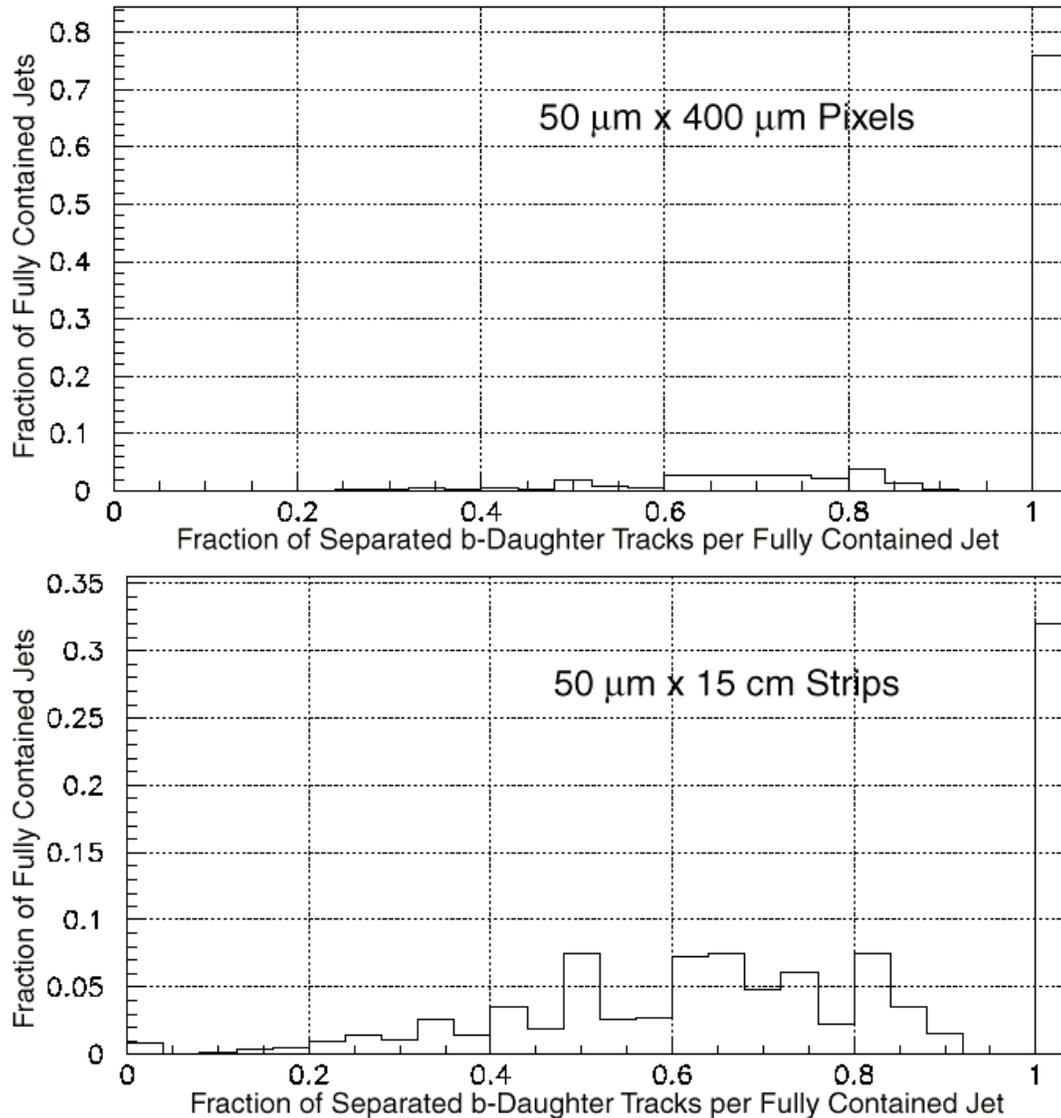
Oct 2003: Ready for data

Initial CDF groups: FNAL, UC Davis, CMU,
New Mexico, Rutgers, LBNL, Purdue, +others
(new institutions, new assistant professors).

*Need to begin FY01 R&D activities starting early
next year with the endorsement of the collaboration
that pixels are part of the baseline RunIIb plans*

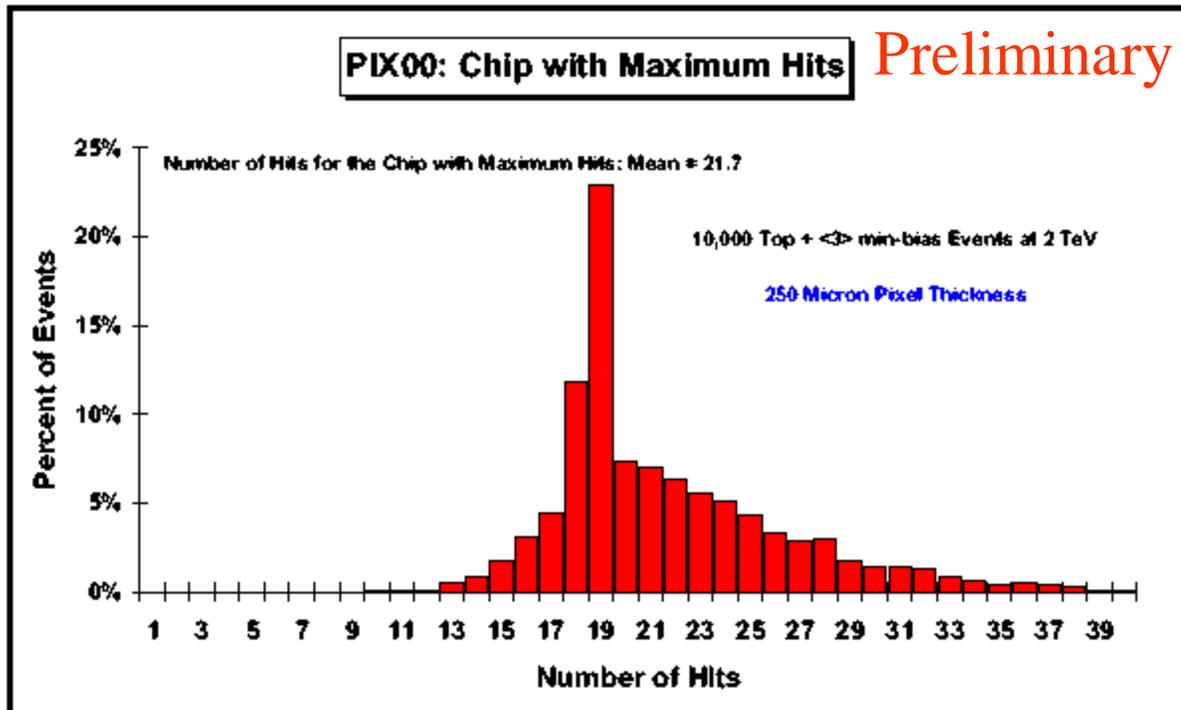
Some Studies

Top + $\langle 3 \rangle$ MB



Geometry study: $>70\%$ of top events have every track separated with pixels and $\sim 30\%$ for strips
Radii fine for pattern recognition

Some Studies



Geometry based study showing in busy top events, the busiest chip has $< 2\%$ occupancy (Layer00 strip study shows top events often have an SVX3 chip with $> 25\%$ occupancy.

40 hits x (safety factor) is not a problem for readout \rightarrow faster than SVXII

Steady min bias rate (< 1 hit) not a problem

Conclusions

- Next studies will incorporate cluster model and thresholds
- Studies of b -tagging are proceeding
 - Overlapping tracks not a problem
 - Pattern recognition and low noise reduce spurious hit assignments
 - SECVTX uses 3 tracks in 2D. With pixels, you might gain 2 tracks in 3D
- Reasonable and Feasible
 - Ask PAC to endorse FY01 R&D plan
 - Jan 2001 for CDF endorsement
 - Approval by the lab a year from now
 - Combined CDF/D0/BTeV effort
 - FNAL and CDF expertise in place