

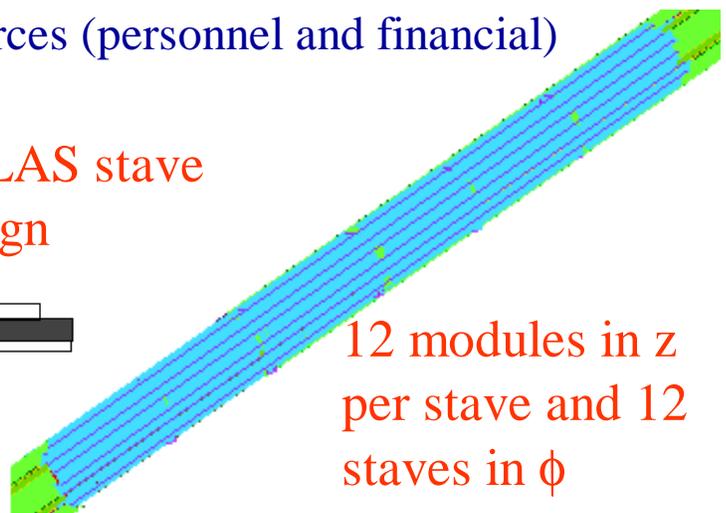
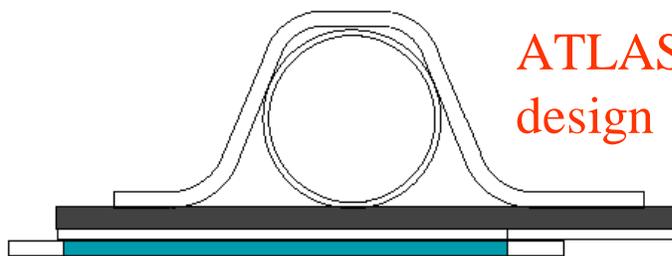
# Pixels for CDF/D0 in Run IIb

Feb 7, 2001 meeting

1. Overview
2. FPIX2
3. Sensors
4. Mechanical
  1. Geometry
  2. Cooling
5. DAQ

# Overview

- Replace Layer00 strips with pixels
  - radiation survivability to 30 Mrad / 30 fb<sup>-1</sup> is desirable
  - pattern recognition: 3.3 M channels vs 14 K channels
  - z resolution 120  $\mu\text{m}$  possible
  - large S:N helps r- $\phi$  resolution, trigger, etc.
  - keep Layer00 strip option a fallback
- Pixels can be ready for 2004
  - ATLAS-style sensors in production
  - FPIX readout chip in advanced prototype
  - cost and schedule fits into RunIIb plans
- Overlap with BTeV and D0
  - BTeV 10% scale test is comparable
  - Economy of scale (preproduction/production quantities)
  - Initial sharing of resources (personnel and financial)



# PAC Presentation

- Run 2b silicon working group
  - Report to CDF review committee
  - Report to PAC
  - Presentation by Michael Schmidt to the PAC on behalf of the review committee
- See CDF Note 5425 and  
[http://www-cdf.fnal.gov/run2b/Run2b\\_silicon.html](http://www-cdf.fnal.gov/run2b/Run2b_silicon.html)
- PAC comments:

The possibility of using pixels in the innermost layer is an intriguing option mentioned by both collaborations. The Committee urges them to work closely with the Fermilab pixel group, building on the success of this R&D program.

# FY01 Requests

- Mechanical
  - ENGINEERING SUPPORT
  - System level mock-up
  - Prototype stave
  - Cooling test
- Electronics
  - ENGINEERING SUPPORT
  - DAQ test stand
  - Progress with RHVD R&D

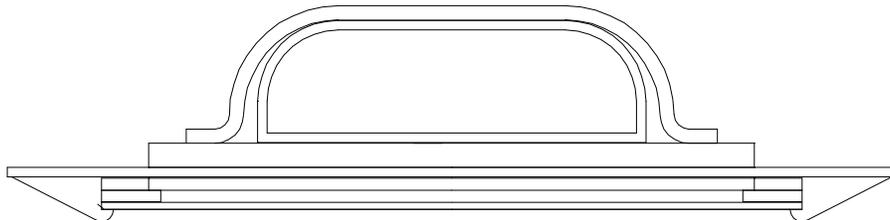
Item	Estimated Cost k\$	Contingency	Total Costs
DAQ Test stand	15	7.5	22.5
System Mechanics	20	10	30
Staves prototypes	20	10	30
Cooling	15	7.5	22.5
Total M&S	70	35	105
Mech. Engineering (FTE)	1.0	0.5	1.5
ESE	0.5	0.25	0.75
Design	1.0	0.5	1.5
Technician	1.0	0.5	1.5

# Electrical Progress

- FPIX chip
  - Pre-FPIX2-T2 works! (last prototype)
  - Gate rupture radiation testing
  - FPIX1 wafer scale testing
  - Initial meetings on FPIX2 finalization for the periphery
- Sensors
  - Discussions with Sally Seidel
  - Engineering available in March for sensor layout
  - Non-disclosure agreement to be discussed by ATLAS on Feb 19
- Both chips and sensors are on track for production order this year

# Mechanical Progress

- ATLAS style stave design
  - Baseline concept
- Mike Hrycyk (SiDet)
  - 3D modeling shows difficult geometry
  - Some preference for carbon fiber shell
  - CERN visit with project engineers
  - Pixels integrated with rest of RunIIb Si
- Possible new chip geometry
  - 256 rows x n columns (n might be 22)
  - Driven by BTeV considerations



# Cooling

- ATLAS cooling aggressive (something like 150 W/stave)
- New power budget is ~500W (40-50 W/stave)
  - Readout chips: 288 W
  - Leaky sensors: 86 W
  - Data lines (1 ohm): 24 W (max)
  - Power lines: 45-140 W
- Goal was use current CDF cooling system (H<sub>2</sub>O-glycol)
- Greg Derylo (SiDet) has performed some initial calculations
  - Laminar flow of current system prevents heat flow into coolant. T~20C
  - Looking at other options such as the fluorocarbon that CMS will use

# DAQ

- Carnegie Mellon, Johns Hopkins, FNAL ESE, and Rad Hard Vertex groups involved.
- Engineer supported beginning in May
- Two basic options
  - Low speed transmission directly from FPIX to DAQ
  - High speed transmission to a port card
  - Token scheme
  - Make progress on DAQ design
- Pixel-FIB board looks straight forward
- ESE group has developed a PC based pixel test stand