

PIX00: A pixel system at the inner radius of CDFII for Run IIb

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1 Pixel Option for L00

1.1 Overview

An option exists to replace the CDF L00 silicon micro-strip detector with a pixel detector. This option makes use of advanced R&D by the LHC experiments and the BTeV experiment. The proposal is to form a single layer of pixels around the beam pipe using ATLAS-style sensors. The sensors will be bump-bonded to FPIX readout chips. ATLAS sensors are in production and the FPIX readout chip, developed at Fermilab, exists in an advanced third generation prototype. In fact, a prototype system (ATLAS-style sensors + FPIX chips) was successfully tested in a December 1999 test beam run at Fermilab using CDF SVX readout electronics (STAR+VRB). Position resolution better than $10 \mu\text{m}$ was demonstrated. The fact that R&D is far advanced makes the order of production chips and sensors in early FY2002 realistic and is a key to the feasibility that this project can be completed by 2004.

The proposed geometry includes 12 staves each 75 cm long and about 1 cm wide. The staves are arranged 12-fold in ϕ to form a long single barrel layer. A staff consists of 12 sensors laid end-to-end with each sensor read out by 8 FPIX chips. The detector comprises 144 sensors and 1152 readout chips. An individual pixel is small: $50 \mu\text{m} \times 400 \mu\text{m}$. In total, the detector contains 3.3 M channels.

The FPIX readout chip has an architecture that is different than the SVX3 silicon strip readout chip. The chip is organized into 18 columns of 160 rows. The FPIX chip makes use of the fact that multiple hits on the same pixel are exceedingly rare. Hence, hits are stored within each cell and logic controls the readout column-by-column. Each cell digitizes the charge collected (3-bit ADC) and holds onto a beam crossing number (BCO) that is associated with each hit. Every hit is read out. For the CDF pixel system, a new DAQ module, the pixel-FIB, would need to be designed to receive all the hit information into a deep memory. The module would then time order all the hits, associate the BCO with a Level 1 accept trigger signal, and provide the pixel information to a VRB for readout. A concept also exists that this module would combine pixel hits into effective strips and send this information to the SVT trigger module.

1.2 Physics Motivation and Tracking Performance

For a Standard Model Higgs discovery and for discovery of several types of SUSY signatures, b -tagging efficiency is very important. Pixels provide excellent position resolution (5-9 μm depending upon the incident track angle) in $r-\phi$. Fig. 1 shows the achieved resolution in the December 1999 test beam run. In addition, pixels provide several other attractive features. First, pixels provide fine segmentation in z that can be used to enhance pattern recognition. Second, pixels provide a precision z measurement that could have a resolution better than $400 \mu\text{m}/\sqrt{12}$. Third, pixels are more tolerant to radiation ($\sim 30 \text{ Mrad} \equiv 30 \text{ fb}^{-1}$) and would require only the single installation even if the accelerator delivers luminosity exceeding current expectations of 15 fb^{-1} . Fourth, pixels have a signal-to-noise that is approximately a factor of 5 larger than with strips.

1.2.1 Track Separation and Pattern Recognition

In the dense cores of jets, the SVX detector and reconstruction algorithms are unable to resolve all tracks. This imposes a limitation on track reconstruction and the identification of secondary vertices in b jets, particularly in high p_T jets from top decay. The charge distributions from tracks in adjacent strips in $r-\phi$ will not be resolved even though the tracks may have z separations of the order of millimeters. The displacement of the charge centroid due to the second track causes measurement degradation in 20-30% of tracks in such jets and leads to spurious impact parameter measurements [1].

We have made a preliminary estimate of the potential for pixels in the innermost layer to cope with the density of tracks in high p_T b jets. PYTHIA [2] was used to simulate b jets from $t\bar{t}$ production at the Tevatron. Tracks from an average of three additional minimum bias interactions were also included with each event. Charged b daughters were selected in a cone of $R < 0.4$ about the direction of the b jet. The generated tracks were extrapolated through a thin cylindrical surface of 15 mm radius and 75 cm length which was either divided into $50 \times 400 \mu\text{m}^2$ pixels or $50 \mu\text{m} \times 15 \text{ cm}$ strips. For pixels, a b daughter track was considered to have an overlap if another track passed through the same pixel or any of its eight neighbors. For strips, only the same or adjacent strips in $r-\phi$ were considered to be overlapping. Note that many of the b daughters we consider in this track density study would not fall within the η or p_T acceptance of the rest of CDF tracker. Also, the overlaps were purely geometric. Charge sharing with adjacent pixels or strips was not taken into account, nor was an attempt made to resolve overlapping tracks on the basis of deposited charge distributions.

Normalized histograms of the fraction of separated b daughters (those without overlaps) for jets fully contained in the cylinder are shown in Fig. 2 for the pixels and in Fig. 3 for the strips. All the tracks were separated by the pixel array in 76% of the jets, whereas for the strips, 32% of the jets had all tracks separated.

As a further comparison, Fig. 4 shows the fraction of fully contained b jets accepted in the pixels and in the strips for various cuts on the maximum fraction of tracks with overlaps.

A distribution was made of the distance in z to the closest potentially overlapping track (*i.e.*, within 100 μm in $r-\phi$) for charged b daughters. The integral of this distribution, Fig. 5, provides a measure of the effectiveness of the pixels to separate tracks in b jets as a function of pixel length.

This preliminary simulation shows the potential for pixels at the innermost radius to resolve a substantial number of b daughters in high p_T b jets which would overlap in a strip detector. Of course, the finite sensor thickness and proximity of the planar sensors to the

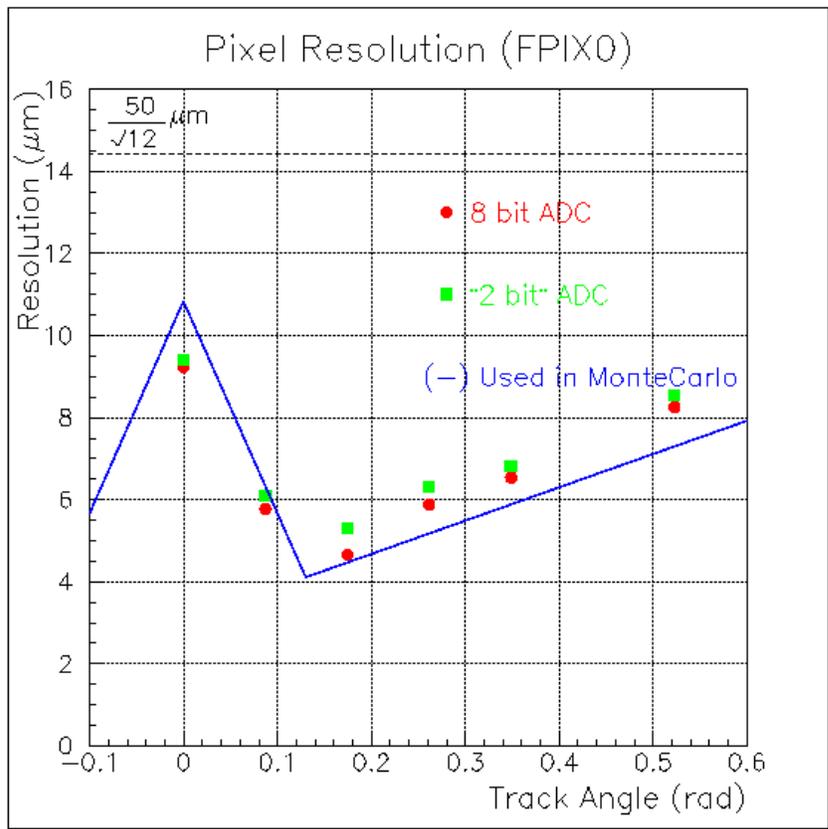


Figure 1: Position resolution of a prototype pixel system versus track angle. These results were obtained from data collected in a December 1999 test beam at Fermilab using prototype ATLAS-style pixel sensors and prototype FPIX readout chips.

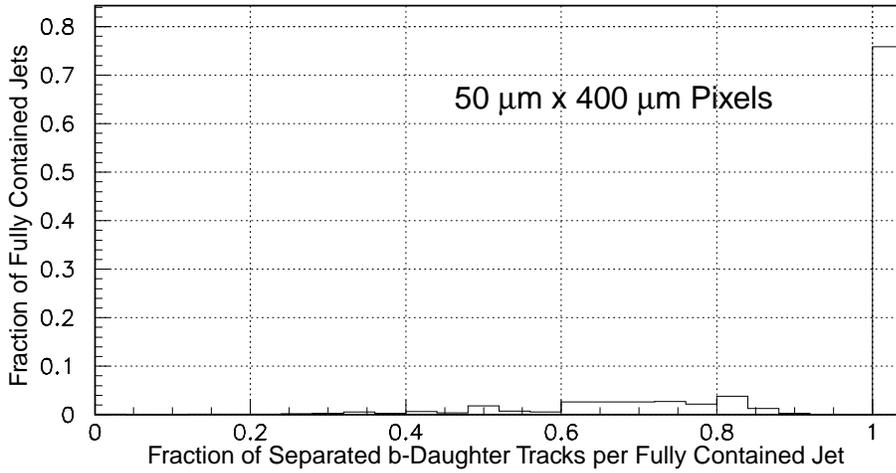


Figure 2: Normalized histogram of the fraction of tracks in fully contained b jets which are separated by a 15 mm radius cylinder of thin $50 \mu\text{m} \times 400 \mu\text{m}$ pixels.

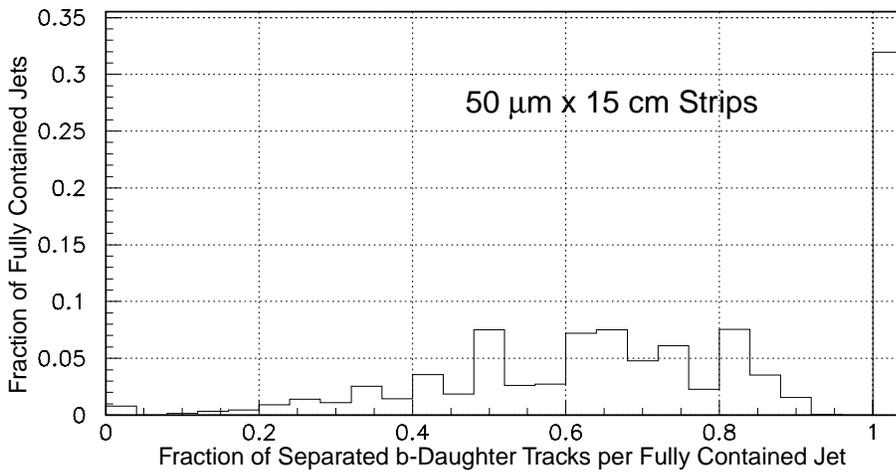


Figure 3: Normalized histogram of the fraction of tracks in fully contained b jets which are separated by a 15 mm radius cylinder of thin $50 \mu\text{m} \times 15 \text{cm}$ strips.

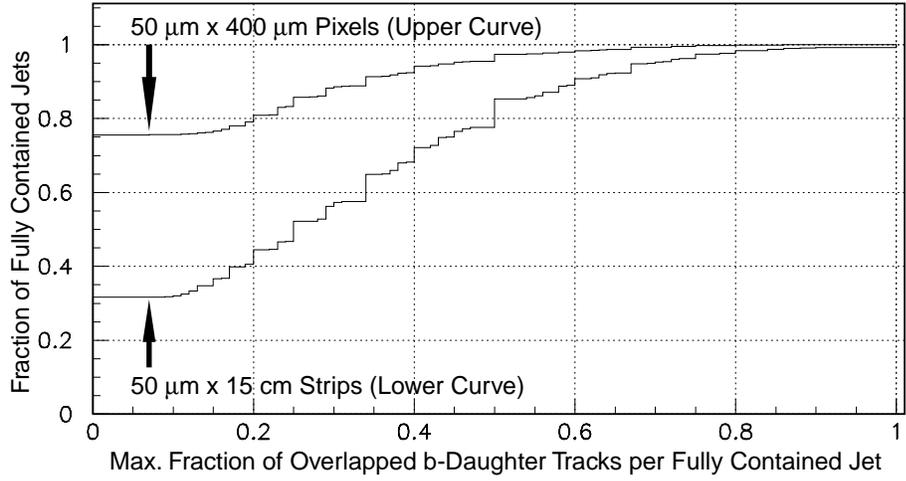


Figure 4: Fraction of jets accepted vs. the cut on the maximum fraction of overlapped tracks in fully contained b jets for a thin, 15 mm radius cylindrical surface of pixels (upper curve) or strips (lower curve).

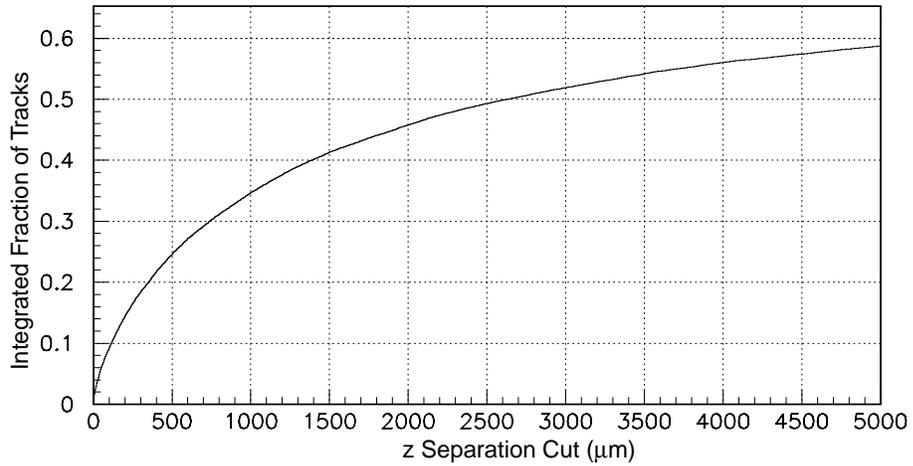


Figure 5: Integral distribution of b jet tracks with nearest overlapping track within the specified z separation cut.

beam will result in tracks depositing charge in some of the adjacent pixels. A more realistic simulation is being developed, taking into account the details of the charge deposition in the sensors and incorporating the pixels into the rest of the CDF tracking simulation. A clustering algorithm must also be developed to resolve nearby tracks and find the best estimate for the hit positions. Here, we can make use of similar work being done by the CMS and BTeV pixel groups who have succeeded in modeling test beam data in terms of cluster distributions.

1.2.2 Precision resolution in z

Pixels also provide a precision measurement in z that is not present with a single layer of L00 strips. The approximate resolution (no charge sharing in z) would be $400 \mu\text{m}/\sqrt{12} = 115 \mu\text{m}$. It is also possible to arrange the pixels in a “bricked” pattern such that those hits that are shared would have an approximate resolution that is better by a factor of two or $58 \mu\text{m}$. The improvements in tracking with this added capability have not yet been fully quantified.

1.2.3 Radiation tolerance

There are large uncertainties in the actual dose expected at the L00 radius in Run 2a. An approximation is that $1 \text{ fb}^{-1} \equiv 1 \text{ Mrad}$. CMS style strips at L00 in Run 2a are expected to last for 10 fb^{-1} whereas ATLAS-style pixels are expected to last to 30 fb^{-1} . Both the design of the pixel sensor and the FPIX readout chip have been tested satisfactorily at radiation doses equivalent to 30 fb^{-1} . In short, at the L00 radius, the radiation environment is very similar to the LHC environment. Pixels are the best technology choice at this time for providing high precision tracking in such a high radiation environment.

1.2.4 Signal-to-noise

The signal due to the passage of an ionizing charged particle through either a strip or pixel sensor is approximately the same ($20,000 e^-$) and is proportional to the thickness of the sensor. Noise is usually dominated and proportional to the capacitance of the strip or the pixel. For a strip detector, a typical S:N $\sim 10:1$ while a pixel detector has a typical S:N $\sim 50:1$. Among other advantages, a large S:N aids in the precision of the $r - \phi$ measurement since better cluster centroid finding can be achieved. The limit of the $r - \phi$ resolution in pixels is dominated by the fluctuations in the Landau charge distributions rather than by noise or other factors.

1.3 Sensors

ATLAS has chosen pixel sensor technology that has achieved high performance out to about 30 Mrad of radiation dose. The $50 \mu\text{m} \times 400 \mu\text{m}$ pixels are composed of n^+ -type implants on n -type bulk with a p-spray isolation. A series of guard rings is also employed. The end result is a sensor that after type inversion and 30 Mrad of dose can use a 600 V bias to collect approximately 2/3 of the charge that is collected by an un-irradiated sensor.

The ATLAS experiment has selected two vendors (CiS and Tesla) to produce their needs of about 1000 wafers of sensors. Each ATLAS wafer contains three sensor tiles that are meant to be bump bonded to two rows of eight readout chips (16 chips total). The CDF pixel system would require about 50 wafers assuming a yield of 50% or 100-150 total wafers if sensors are shared between D0 and/or BTeV. Each wafer would contain six sensor tiles that

are meant to be bump bonded to a single row of eight chips. It is reasonable that sensors with the ATLAS-style specifications could be ordered with a CDF-style geometry in the Fall of 2001.

The CDF University of New Mexico group leads the ATLAS pixel sensor development and testing. This group has facilities that will be available (with minimal impact on their ATLAS commitments) for sensor probing and module tests for acceptance and characterization.

1.4 FPIX readout chip and DAQ

The Fermilab rad hard vertex group has worked with the BTeV group and Ray Yarema's ASIC design group to develop a pixel readout chip that is suitable for use by experiments at the Tevatron. It is anticipated that a CDF pixel system could use a readout chip which is either identical to or only slightly different from the one being developed for BTeV. The current prototype version of the chip has a final design core (amplifiers and digitization for each pixel cell) already qualified in a deep submicron process ($0.25 \mu\text{m}$). Radiation testing at a Co-60 facility to 30 Mrads shows little or no degradation. A next prototype has been submitted at the end of September 2000 and contains a periphery that tests several options for communication between the pixel chip and the DAQ. This prototype also takes a big step towards final design by deriving all internal voltages off of a single supply voltage. The FPIX readout chip development has gone very well. In some sense, by choosing early to use a deep submicron process, the FPIX chip is more advanced than the LHC pixel readout chips. It is reasonable that production chips could also be ordered in the later part of 2001.

The FPIX chip has a different readout scheme compared with the SVX3 chip. In particular, pixel hits are stored within each pixel cell with a beam crossing number, BCO. Every hit gets read out with row and column information, the BCO, and 3 bits of digitized analog information. The concept is that the pixel detector will send all the data to a deep memory module that will sort pixel hits by BCO and will match L1 accepts with the correct BCO. The module will then provide pixel data to a VRB module for readout. A concept also exists for this module to combine pixel hits back into effective strips to provide data to the SVT with no hardware changes to the SVT. This deep memory module will also provide the control signals to the FPIX chip (it is equivalent to the FIB module). The deep memory/pixel-FIB would be a new module that would need to be developed. The control of the FPIX is simpler than SVX3 so the scale of producing this module is estimated to be equal to the scale for FIB development.

Various other aspects of the pixel DAQ including a pixel port card have been under development for BTeV studies within the same Fermilab ESE group that designed the SVX DAQ. The pixel port card would be expected to contain commercial optical drivers and would sit outside the tracking volume in a not-so-intense radiation environment. A HDI cable would connect FPIX chips on the sensors with the port card. Prototype components of this DAQ are currently under test by the ESE group.

A study has begun to examine the maximum pixel chip occupancy in busy top events in order to identify potential problems or DAQ limitations. In particular, the number of hits in a single pixel chip in busy $t\bar{t}$ events for the chip with the maximum number of hits is a figure of merit. Preliminary studies suggest the occupancy of the busiest chip is almost always below 2%. These hits should be able to be clocked out at 25 MHz (conservative estimate) in a total of $2.3 \mu\text{s}$ which is small compared with the $5.5 \mu\text{s}$ 42-deep 132 ns pipeline in the SVX3 chip. Our plans are not only to continue the occupancy studies but also to provide

the output of the simulation into a Verilog model of the FPIX chip so that detailed timing issues can be predicted.

1.5 Bump Bonding

Hybridization, or flip-chip bump-bonding (the bonding of the sensor chip to the readout chips in a pixel detector), has been studied for some years by the UC Davis group and by ATLAS and BTeV. Three vendors have been qualified, or nearly qualified, to perform the hybridization for ATLAS. They are all in Europe. Their choice of technology is either that which uses indium for the bump material (two vendors) or Pb/Sn solder (one vendor). A fourth vendor, MCNC-Unitev, is in the U.S. and is under investigation by CMS and BTeV. This vendor uses Pb/Sn. In addition, UC Davis has facilities for the complete process of depositing indium bumps and bonding the chips to the sensors. They also are capable of carrying out the process for a single chip, something that is expensive and time-consuming when done by commercial vendors, if one can be found that is willing to do it. Prototype chip development typically is done at the chip level, not the wafer level, so one has to be able to bond single die and sensor chips. UCD has done this for several users, most recently for the US CMS beam tests at CERN, as well for their own pixel beam tests at SLAC.

The costs of commercial hybridization are not yet well defined for the size of job represented by a Run 2b pixel upgrade. Cost estimates in 1998 for a set of pixel detectors with about 4,300 chips were roughly \$350,000. Linear scaling to a smaller number of chips would not be valid, but sharing with BTeV, for example, could reduce the cost below that of an independent submission. Having UCD do the hybridization would very likely be the least expensive route, but no serious estimates of that cost and schedule have yet been made.

1.6 Mechanical Design, Cooling, and Material Budget

A pixel detector module for CDF would consist of an 8×64 mm² silicon sensor with 8 bump-bonded readout chips. A Kapton hybrid circuit would be attached to the top of the sensor to bus signals to and from the readouts via wire bonds. The wire bonds could be encapsulated to prevent damage by interconnecting cables. The pixel size would be $50 \mu\text{m} \times 400 \mu\text{m}$.

Similar modules have been successfully constructed and tested in the Fermilab FPIX program using ATLAS sensors and FPIX readout chips. Fig. 7 shows 5 FPIX chips bump bonded to an ATLAS sensor, which is designed to be read out by 16 chips in two rows. As stated above, the CDF pixel modules would have one row of 8 chips. A test board is shown in Fig. 7. The readout chips are underneath the sensor with their bond pads extending beyond its edge. The Kapton flex circuit is also attached to the board in this prototype. At a later stage, the chips will be connected to a narrower flex circuit mounted on top of the sensor, as in the final design.

The mechanical support and cooling structure is based on the relatively mature ATLAS design. It consists of a barrel made of 12 “staves” holding 12 detector modules each. The active length of each stave is approximately 75 cm, which is shorter than the ATLAS staves (1 m). A cross section of a stave is shown schematically in Fig. 8. The stave includes a long carbon-carbon heat conducting bar to which the detector modules are attached. A thin-walled aluminum cooling pipe runs the length of the bar and is held in place by a carbon fiber-epoxy “omega” channel which provides rigidity. Thermally conductive grease is used to provide thermal contact between the aluminum tube and the carbon-carbon bar. The bar, omega channel and silicon detector module have similar CTEs. The CTE of the aluminum

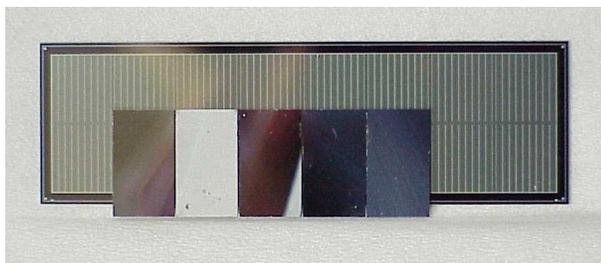


Figure 6: FPIX chips bonded to ATLAS sensor.

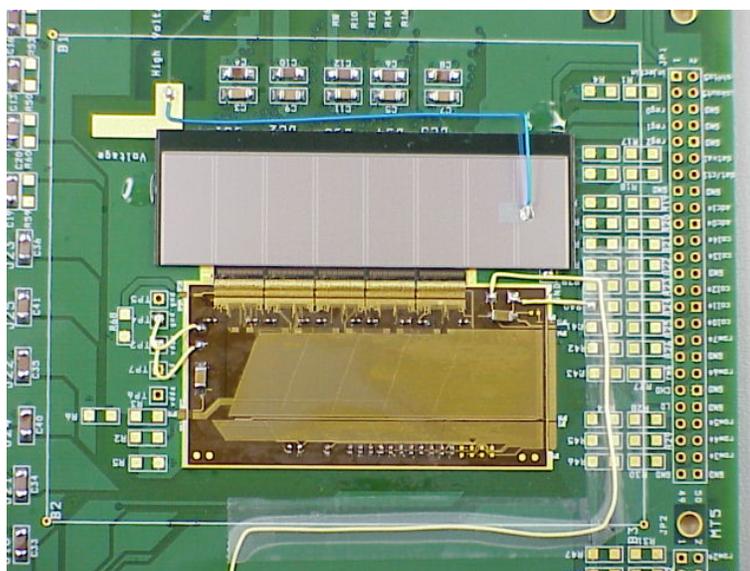


Figure 7: Detector test module with 5 chips wire-bonded to 5-layer flexible circuit.

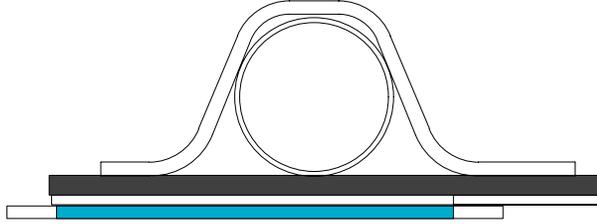


Figure 8: CDF pixel detector stave concept (cross section). The active area of the sensor is shown in color.

tube is sufficiently different that it must not be rigidly attached to the bar.

The ATLAS staves are supported at the ends and center by a carbon composite cylinder at a larger radius. In our case, we envision that the beam pipe would be used for support.

Two possible configurations of the staves to form a barrel layer (tilted or staggered) are shown schematically in Fig. 9 and Fig. 10, respectively. The 10° tilt partially compensates for the Lorentz angle of the charge carriers in the sensors. The tilted design also interposes less material on average between the beam pipe and the first sensor layer. The barrel staves must be positioned to avoid contact with the “flag” on the underside of the beam pipe.

The Kapton cables to connect the detector modules to the outside world are attached to the surface of the hybrid circuit and routed tangentially outward to the region outside the barrel layer where they make a right angle and proceed along the barrel next to the omega channel of the neighboring stave.

1.6.1 Cooling

The power dissipation of the FPIX chips is quite high and an adequate cooling system is required to keep most of the pixel system at low temperatures. The core of the pixel chip generates $55 \mu\text{W}$ with about an additional 20% in the periphery expected. In short, the entire pixel detector is expected to generate 250 W. The ATLAS stave design assumes a somewhat higher power dissipation by area and uses twice as many chips per unit stave length. They found that 2 mm radius cooling tubes were sufficient for their design, which also includes other complexities in terms of the coolant and distribution. We are hopeful that a simpler design using cooling tubes not much larger than 1.5 mm in radius will be more than adequate. We are in the process of simulating our heat generation and cooling scheme to confirm these expectations.

1.6.2 Material Budget

An important design constraint for any precision tracker is to keep the amount of material in the active volume as low as possible. Material estimates for ATLAS and BTeV modules are 0.7% of a radiation length excluding cooling and support. For the ATLAS stave design, the material in a stave is estimated to be 1.59% of a radiation length. In our design, we use similar materials and thicknesses (including $250\mu\text{m}$ thick sensors and $200\mu\text{m}$ thick readout chips). However, our geometry has larger overlap between adjacent staves such that we expect the average over ϕ of our detector will be slightly thicker in terms of radiation length. In both the staggered and tilted geometries, you will notice that areas that have four thicknesses of silicon are in regions without cooling. Regions with the additional cooling material generally have fewer layers of silicon. This design helps make the material distribution more uniform

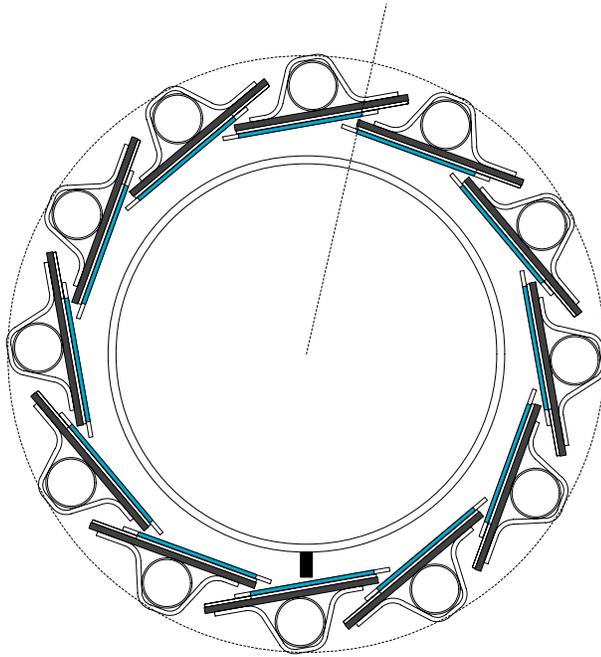


Figure 9: CDF tilted stave configuration (10° tilt).

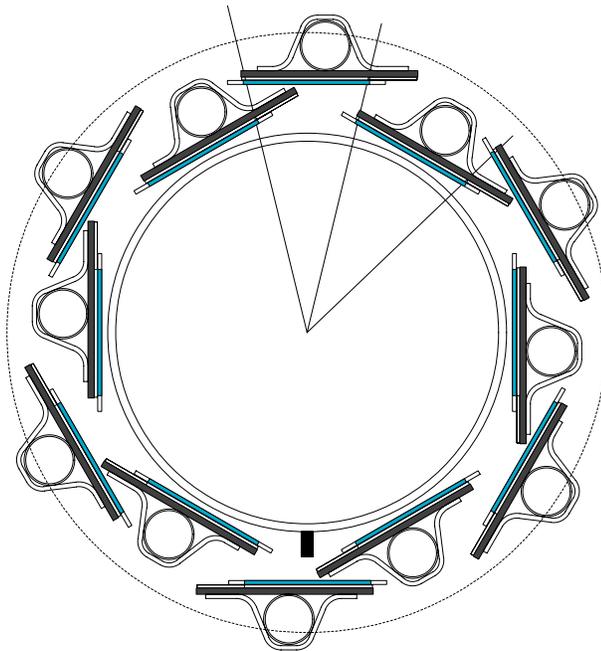


Figure 10: CDF staggered stave configuration.

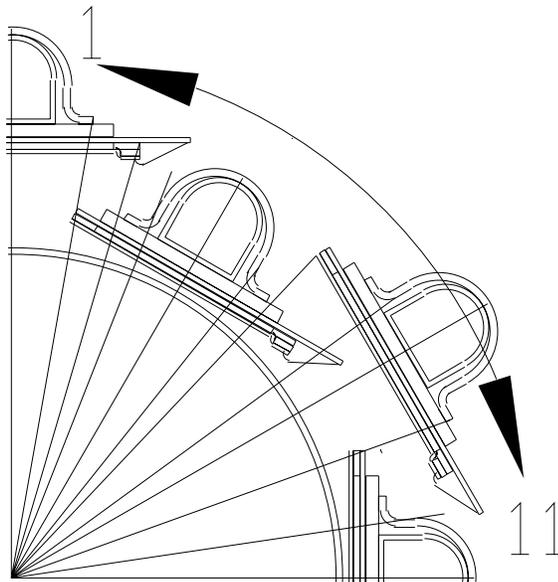


Figure 11: A quadrant of the pixel detector showing eleven regions in ϕ for which the amount of material has been estimated.

in ϕ . Fig. 11 shows a schematic of a quadrant of the pixel detector with eleven regions in ϕ shown. Tab. 1 lists the fractional area of each of the regions and the estimated effective thickness of various materials. The total average radiation length of 1.87% from this study is below an initial goal of keeping the material below 2.5% X_0 . Other materials such as bonds, grease, and glue are not expected to contribute substantially. Possible overlapping of HDI cables has not been taken into account. Each HDI cable adds about 0.1% X_0 so that, at most, an additional 0.6% X_0 would be in front of the modules at the ends. An initial study shows that very little degradation in impact parameter occurs even if 2.5% X_0 material is compared with 1.5% X_0 of the current L00 design.

1.7 Resource and Cost Estimates

The resources and costs needed for completing this project are greatly reduced due to the substantial overlap with this project and BTeV's proposed 10% scale test. For this discussion, we assume that both this proposal and a 10% BTeV test are approved (D0 is also considering a pixel option that is nearly identical to this proposal). Table 2 shows our initial cost estimate. The amounts were mostly derived from the BTeV cost proposal and from CDF experience with its Run II silicon system. Contingency of 50% is assumed (30% contingency on sensors, readout chips, and pixel-FIB). In round numbers, the cost to CDF of this project (assume engineering costs are absorbed by FNAL and universities) would be \$1.5M (\$2M if there were no cost sharing with BTeV, and \$1M if CDF, D0, and BTeV all shared costs).

In particular, we make several assumptions. For the sensors, we use costing numbers based upon the ATLAS submission (the actual order costs are not public) of \$25K for setup including masks and \$1K per wafer in quantities of several 10's (BTeV production costs were \$2.5K per wafer). For the FPIX chips, CDF would require about 10 wafers. BTeV would similarly require 10 wafers. These wafers cost \$161K for the first ten and only \$32K for each additional ten. These examples demonstrate the economy of scale if more than one

Region	%	Si	kapton	Cu	C fiber	Al	H ₂ O/Glycol	Alumina	X/X ₀ (%)	Tot.
	X ₀ (mm)	93.6	284	14.3	220	89	361	72		
1	11.2	450	200	3	1000	400	2000	0	2.03	0.23
2	7.0	900	400	46	400	0	0	120	1.77	0.12
3	5.6	650	200	43	700	0	0	0	1.38	0.08
4	9.6	450	200	3	1000	400	2000	0	2.03	0.19
5	9.2	450	200	3	1000	400	2000	0	2.03	0.19
6	6.1	450	200	3	700	0	0	0	0.89	0.05
7	10.1	900	400	46	400	0	0	120	1.77	0.18
8	7.9	450	200	3	1000	400	2000	0	2.03	0.16
9	11.3	450	200	3	1000	400	2000	0	2.03	0.23
10	12.6	900	400	46	700	0	0	120	1.91	0.24
11	9.4	450	200	3	1000	400	2000	0	2.03	0.19
Total										1.87

Table 1: Material estimate for a pixel detector for CDF. Shown is the effective thickness of various materials (in μm) in eleven ϕ regions. The percent of a radiation length for each region is tabulated as well as the contribution of each region to the average of the total.

pixel project overlaps. The bump bonding costs are derived again from BTeV's estimates based upon commercial costs and are substantial. As discussed above, UC Davis has bump bonding capabilities and could perform the production bump bonding. If the bonding is done at UC Davis, there could be cost and schedule savings; however, some funds would be required to provide support for necessary tooling and for technician labor. The construction of modules has been costed assuming that there is no overlap with the BTeV R&D. However, it is possible that for the BTeV 10% tests, these costs could have a high degree of overlap. Test stand and probe station costs are not included since a number of interested institutions already have those capabilities. Most of the other items have costs estimated either by similar items on the BTeV cost estimate or with other expert discussions. For example, the pixel-FIB costs are estimated to be equal to the SVX FIB modules per a discussion with the Fermilab ESE group.

As far as personnel resources, sufficient resources exist with the Fermilab ASIC design and rad hard vertex groups to see that production sensors and readout chips could be ordered in the Fall of 2001. For the bump bonding, we are examining UC Davis' capabilities or we could follow the commercial lead that the BTeV group chooses to employ. For mechanical and cooling, we require the use of engineers and designers currently at SiDet beginning at the earliest possible time (approx. Jan. 2001). We hope university groups will also play a leading role in the mechanical design of this detector. Details on the FY01 needs can be found in a later section of this document.

This project makes use of the expertise of the Fermilab rad hard vertex group and various CDF institutions actively involved in either pixel or diamond work for the LHC experiments. DAQ and other hardware (HDIs and port cards) have also been made by CDF institutions in the past. We expect support from the Fermilab ESE group who has been involved both on the CDF and D0 silicon DAQ and the prototype pixel DAQ for BTeV.

While more complex detectors have been achieved in this short of a time period (SLD CCD detector, for instance), a pixel detector around the beam-pipe at CDF by 2004 requires an aggressive schedule that has little time for R&D. However, as the R&D has been done on

Description	Quantity			Unit (\$K)	Units	Cost (\$K)	Cost w/ contingency
	Base	Spare	Total				
Sensors NRE	0.5		0.5	25	each	12.5	16.3
Sensors	24	26	50	1	wafers	50.0	65.0
FPIX	1152	1700	2852	0.03	chips	96.0	124.8
Bump bonding	24	14	38	2.9	wafers	110.2	165.3
Module R&D	12		12	4	modules	48.0	72.0
Modules	144	84	228	0.58	modules	132.2	198.4
HDI cables	144	84	228	0.50	cable sets	114.0	171.0
Pixel port card	24	6	30	3	boards	90.0	135.0
High voltage	24		24	3	supplies	72.0	108.0
Low voltage	24		24	2	supplies	48.0	72.0
Monitoring	1		1	20	system	20.0	30.0
Interlocks	1		1	20	system	20.0	30.0
Pixel-Fib	24	6	30	5	boards	150.0	195.0
Opto-electronics	1152	348	1500	0.03	each	45.0	67.5
DAQ cables	24	6	30	1	bundles	30.0	45.0
Staves R&D	2		2	20	each	40.0	60.0
Staves	12	3	15	3	each	45.0	67.5
Stave support	1		1	20	system	20.0	30.0
Cooling manifold	1		1	20	system	20.0	30.0
Cooling system	1		1	20	system	20.0	30.0
Total						\$1,178	\$1,705

Table 2: Preliminary cost estimate for a pixel detector for CDF.

many components, we believe the project is feasible. The proposed schedule is that production sensors and chips arrive by the end of 2001. Year 2001 will also be used to complete the mechanical and DAQ design. In 2002, testing sensors/chips followed by bump-bonding will result in the completion of modules by the end of 2002. Also in year 2002, fixturing and other materials will be ordered for the mechanical construction of staves and the detector. Prototype DAQ modules will also be ordered and debugged. Year 2003 will be devoted to constructing staves and assembly of the final detector including DAQ. The detector should be ready for installation in late 2003 or early 2004. A more detailed delineation of a schedule has been tabulated by D0 who arrived at the same conclusions on a detector completion date by 2004.

1.8 FY01 R&D needs for pixels

In this section, we spell out R&D needs for FY01 for the option to replace L00 with a pixel detector. These needs reflect a constraint on available financial resources; however, they are sufficient provided that activities lead towards the beginning of fabrication in FY02. We first provide an overview of our requirements for personnel and financial resources. We then provide details of what we wish to accomplish in FY01 for CDF pixel electronics and mechanics. Note that many of the FY01 activities on electronics overlap with planned activities by the Fermilab rad hard vertex, ESE, and ASIC design groups. The costs for a pixel R&D program in FY01 is summarized in Table 3.

1.8.1 Personnel needs

We need two mechanical engineers/senior technicians at a level of 25-50%. Presumably these engineers would be located at SiDet. One engineer would oversee conceptual design and mock-up of the larger scale system (mounting on the beam pipe, cable and cooling routing etc.). The other engineer would help coordinate the design of the carbon fiber supports and cooling structures. Resources equivalent to one FTE technician would be required for making prototypes. Designer/drafter support at the level of one FTE is also required. We assume that periodic support from other personnel at SiDet would be available.

For electronics, we require a small amount of support from the Fermilab ESE and ASIC design groups. We believe that activities during FY01 will overlap substantially with BTeV activities so that no additional personnel will be required. CDF physicist involvement in these activities will allow these groups to increase their current FY01 plans to allow for both BTeV and CDF specific work.

1.8.2 Financial needs

We would need a total of \$70K before contingency for the following purposes. For both the FPIX readout chip and for ATLAS-style sensors, we require no additional funds in FY01 (if CDF cannot use the BTeV chip, a CDF specific FPIX prototype would cost \$37.5K – this is not expected to be needed). For a CDF pixel DAQ test stand, we need \$15K for modifying a SVX test stand into a pixel test stand. These funds would also be used to purchase prototype electronic components that are CDF specific. For system level mechanical design, we would need \$20K for the components necessary for a system mock-up and other R&D needed to qualify certain materials and technology choices. We would need \$20K to produce prototypes of carbon support and cooling structures. This includes fixtures and materials for producing

Item	Estimated Cost k\$	Contingency	Total Costs
DAQ Test stand	15	7.5	22.5
System Mechanics	20	10	30
Staves prototypes	20	10	30
Cooling	15	7.5	22.5
Total M&S	70	35	105
Mech. Engineering (FTE)	1.0	0.5	1.5
ESE	0.5	0.25	0.75
Design	1.0	0.5	1.5
Technician	1.0	0.5	1.5

Table 3: Resources required for Pixel R&D in FY01.

the carbon elements. We'd need up to \$15K for materials and equipment used in cooling tests.

1.8.3 Electronics

FPIX chip: We require no additional FNAL resources. CDF will benefit from FPIX prototype submissions and studies carried out by the rad-hard vertex, ESE, and the ASIC design groups. Final decisions on the exact nature of the periphery will be made and tested in these prototypes. There will also be radiation testing of prototype devices to check for resistance to single event upset and single event gate rupture effects. These tests will lead to the final specifications of the FPIX chip. The FPIX road-map is such that a full size chip should be ready for submission in early FY02. This chip could be the production chip; but, the schedule allows for a standard sequence of a preproduction run followed by a production run. In addition, planned R&D in FY01 includes establishing wafer scale testing procedures at Fermilab. By the end of FY01, we should have a prototype FPIX chip in hand that would need only minor changes before the production order can be placed.

Sensors: We require no additional FNAL resources. CDF will benefit from resources earmarked for BTeV to produce prototype sensors. Engineering and CAD work will be done either at FNAL or at a university to transform ATLAS GDS files into CDF sensor designs. The University of New Mexico will provide assistance especially if the "bricked" pixel option is chosen as they have produced prototypes in the past. UNM will also be establishing testing and characterization facilities for the sensors. By the end of FY01, we should have the final design of the sensor ready in appropriate GDS files. The layout of sensors on wafers will be specified if wafers are shared between CDF and BTeV and D0. Early in FY02, production sensors should be able to be ordered.

Bump bonding: We require no additional FNAL resources. UC Davis will be available for prototype bump bonding activities as they have done for other efforts in the past. In FY01, UC Davis will determine whether they wish to be considered for doing the production scale bump bonding for this project. Other FY01 activities include the evaluation and reliability tests of commercial bump bonding with thinned FPIX devices. Prototype modules (discussed below) will also be constructed and will test bump bonding. By the end of FY01, we should have determined the preferred methods for bump bonding readout chips to sensors.

HDI cable: We require no additional FNAL resources. On-going BTeV studies include the evaluation of HDI cables. CDF Run 2b silicon strips also require specialized fine pitch

HDI cables. By the end of FY01, preferred vendors should be selected and prototypes evaluated with near final specifications determined.

Modules: We require no additional FNAL resources. BTeV activities include the construction of prototype “stacks,” several FPIX1 readout chips bump-bonded to a prototype sensor with a wire-bonded HDI. By the end of FY01, the module concept will have been completely prototyped.

Pixel port card (CDF specific): We require minimal additional FNAL resources. BTeV activities include the evaluation of various options for driving FPIX signals and controls between the DAQ and pixel detector. Specifications of this board will be driven by the final design choices of the periphery of the FPIX chip. It is thought that the same concepts for a similar BTeV component will be shared with the CDF pixel port card, but some tests may be necessary to be carried out for CDF specific issues. By the end of FY01, concepts to be used on the port card should have been tested such that prototypes can follow in FY02.

Pixel-FIB (CDF specific): We require minimal additional FNAL resources. This board is thought to be similar in scope to the Run II FIB module. The Fermilab ESE group who designed the Run 2a FIB module and is working on BTeV DAQ issues believes that it can take a lead role in the design and fabrication of this board. Assistance from universities especially with software and testing is also expected. A great deal of work and effort is required on this board in FY01. Some components may need to be purchased for testing. However, most of the work is in the engineering design that incorporates CDF required specifications. By the end of FY01, progress on the design and specifications of this board will allow for prototypes to be produced in FY02.

SVT Interface (CDF specific): We require minimal additional FNAL resources. We require engineering design to best make pixel information available for the SVT. This interface is likely to be incorporated into the pixel-FIB module. This activity will overlap with the development of specifications of the pixel-FIB. Some components may be purchased for tests. By the end of FY01, we should have the concept firmly defined and prototype circuitry designed.

DAQ test stand: We require minimal additional FNAL resources. BTeV activities include the commissioning of a test stand for reading out the prototype module “stacks.” This test stand will test conceptual DAQ features such as differential signal readout followed by optical transmission. A test stand dedicated towards CDF specific activities should also be commissioned. It is expected that there will be some costs associated with this activity. By the end of FY01, a CDF pixel test stand should be commissioned.

1.8.4 Mechanical

The FY01 goals for mechanical issues are to validate the concepts outlined in this document, construct prototypes of the stave elements and a complete system, and begin to produce engineering drawings to be used for the actual construction of the pixel detector.

System mock-up: We do require funds and engineering and technician assistance. This system mock-up will be used to determine outstanding issues associated with the stave concept and other global mechanical issues. Besides a visible mock-up of a pixel detector, by the end of FY01, this activity will lead to concepts and engineering drawings of the support system, cooling manifold, cable routing, etc.

Prototype stave: We do require funds and engineering and technician assistance. The goal is to produce prototype carbon based structures including the C-C plate and the carbon fiber omega-channel. Particular attention will be made to the stave stiffness and environ-

mental effects such as temperature and humidity dependence. By the end of FY01, the construction techniques for staves will be established.

Cooling test: We do require funds and engineering and technician assistance. Cooling the pixel detector both for removing the heat generated by the readout chip and for keeping the sensors cold is critical for the detector. The concept is to use a cooling system based upon ATLAS designs, but simpler. For example, we envision using an aluminum cooling tube within the omega channel instead of relying on a seal between the C-C plate and omega channel. These concepts do require testing and can be done either at SiDet or a university. By the end of FY01, the concept for cooling staves will be finished with calculations of the temperature profile along the staff performed.

1.9 Conclusions and Feasibility

The key points of proposing a replacement for L00 micro-strips with a pixel detector are the following. First, pixels provide precision space points that extend our current capabilities by providing advantages in pattern recognition. Second, pixels are radiation hard at a level required for continuous high luminosity running (no second shutdown for another replacement). Third, a pixel detector at CDF makes use of expertise both at Fermilab within the rad hard vertex group, the ESE group, and SiDet; and makes use of expertise among CDF collaborators engaged in silicon and diamond pixel detector development for other projects. Fourth, the cost of this project to the laboratory is reduced due to the overlap with plans for continued pixel development at the Tevatron and the potential for outside groups to raise money for advanced detector development. A pixel detector is the best technology choice at small radius in the collider detectors and is achievable at a reasonable cost to the laboratory.

1.10 Acknowledgement

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