Pixels in Run IIb

Precision tracking in the high radiation collider environment for a Higgs discovery at the Tevatron before LHC turn-on.

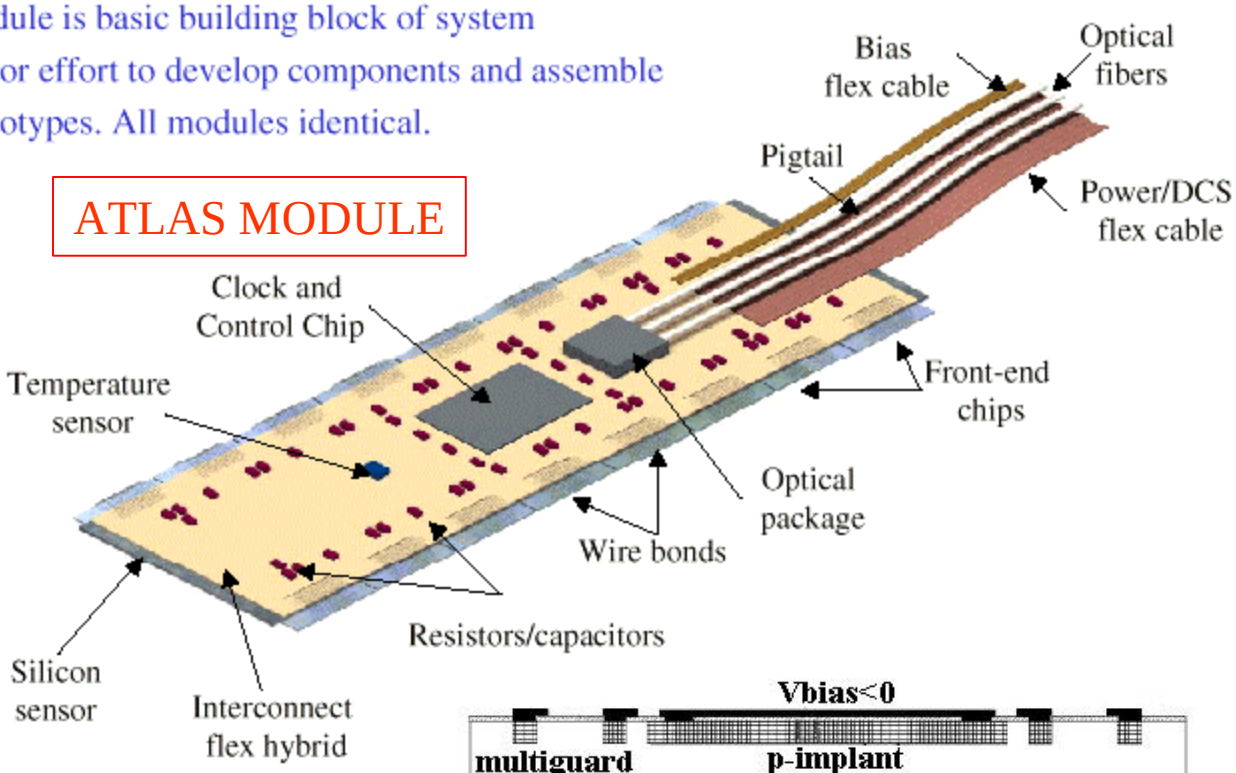
- Pixels provide advantages over other technologies at small radius
  - radiation hard to ~30 Mrad
  - large S/N (noise typically 100 e- or less)
  - pattern recognition
- Pixels are feasible using advanced R&D at FNAL and LHC
- Layer00 replacement strip option to be pursued until clear advantages and schedule non-risk are demonstrated

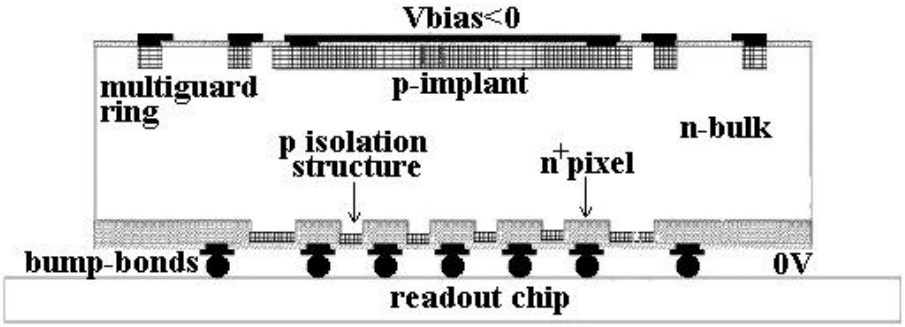
		Outline:
W. Wester	Fermilab	Overview
M. Hoeferkamp	UNM	ATLAS pixel sensors update
R. Yarema	Fermilab	0.25μm FPIX2 chip and beyond
D. Pellet/G. Grim	Davis	Bump bonding/DAQ architecture
G. Bolla	Purdue	Pixel sensor testing
S. Zimmerman	Fermilab	DAQ and readout issues

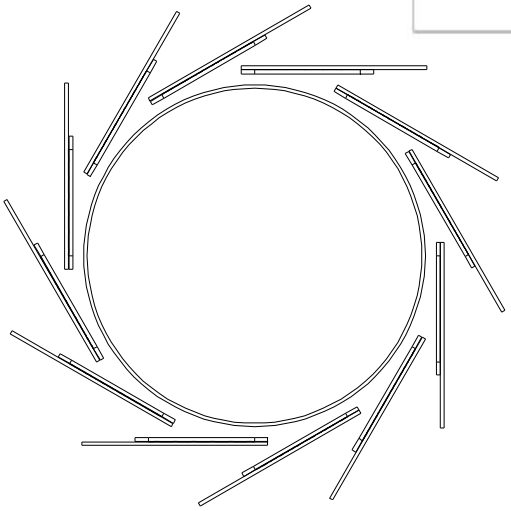
Pixel concept 0

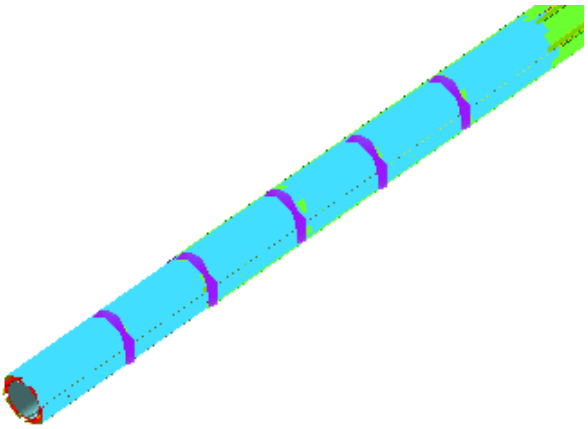
Module is basic building block of system
Major effort to develop components and assemble prototypes. All modules identical.

ATLAS MODULE







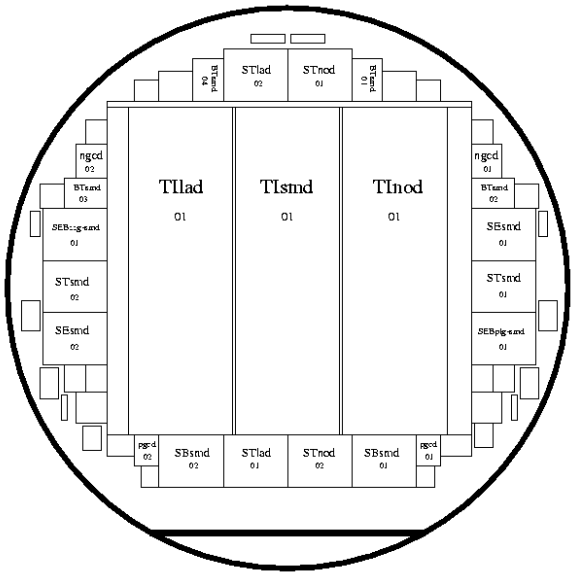


Pixel concept 0

Pixel size: 50x400 µm^2
Die size: 18 col x 160 rows
  active: 0.8 cm x 0.72 cm
  power: 55 µW/pixel

Module size: 8 single row of readout chips
  active: 0.8 cm x 5.8 cm
  at 90 deg, module design is 0.7% rad length
Detector: 12 (phi) x 12 (z) = 144 modules
  active: 70 cm long
Total channels: 3.3 million

ATLAS WAFER



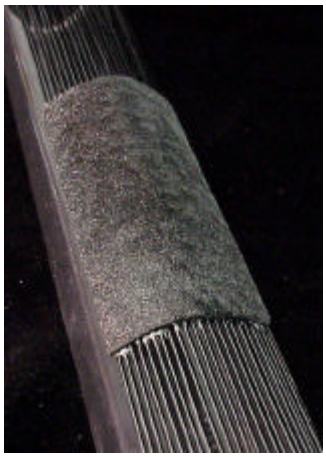
FPIX1 chip

For CDF, up to six sensors per four inch wafer. Only 24 total wafers needed to cover Layer00. Only 1152 readout chips.

The proposed CDF Layer00 replacement overlaps and is on the same scale as the 10% system engineering plan proposed by BTeV.

Pixels are feasible

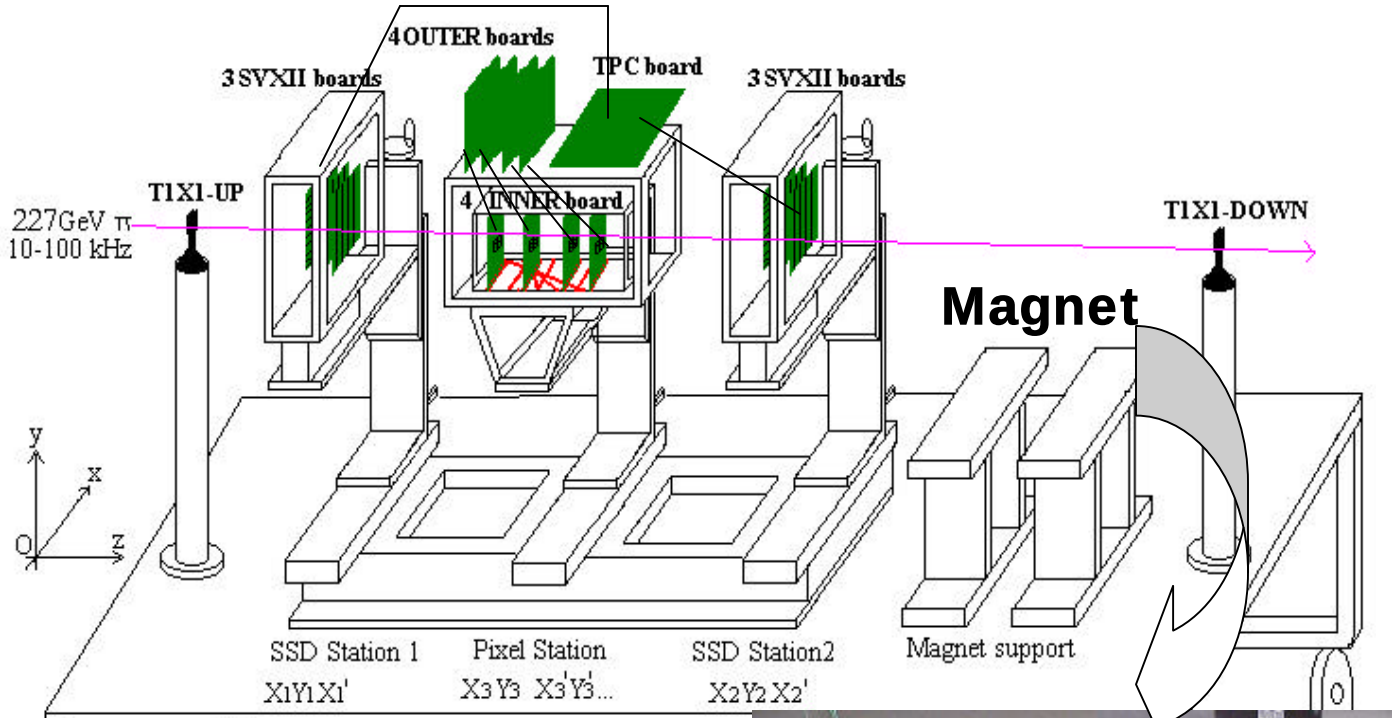
- Use ATLAS style sensor design
- Use FPIX style chip developed at FNAL ("the BTeV chip")
- Use DAQ components that can utilize CDF modules
- R&D on mechanical design shared with single-sided silicon/LHC efforts.

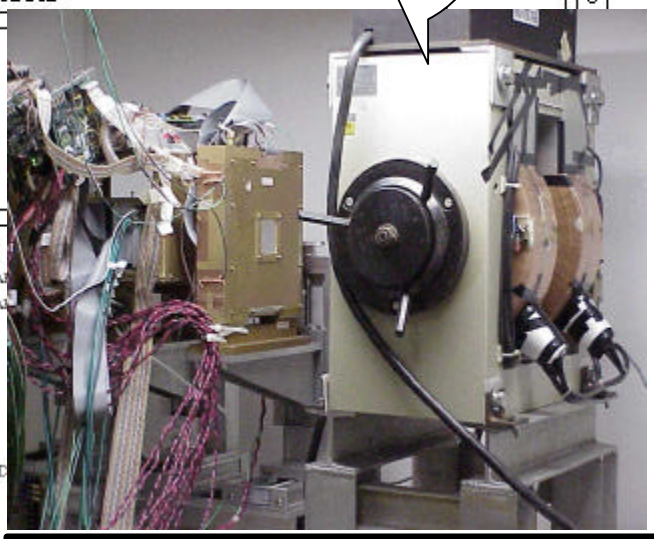


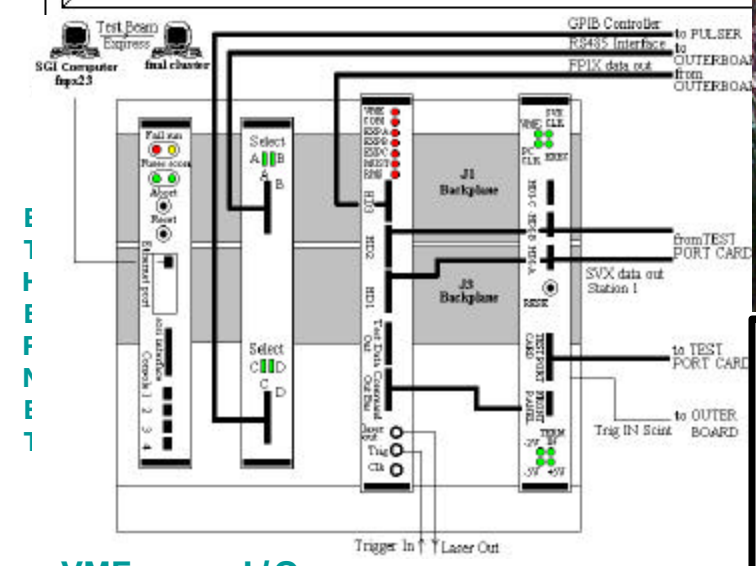
Fuzzy carbon with carbon cooling pipes. Alternative: Be support with machined cooling groove (CMS).

Already demonstrated in the test beam

Pixel Testbeam (courtesy of G. Chiodini)

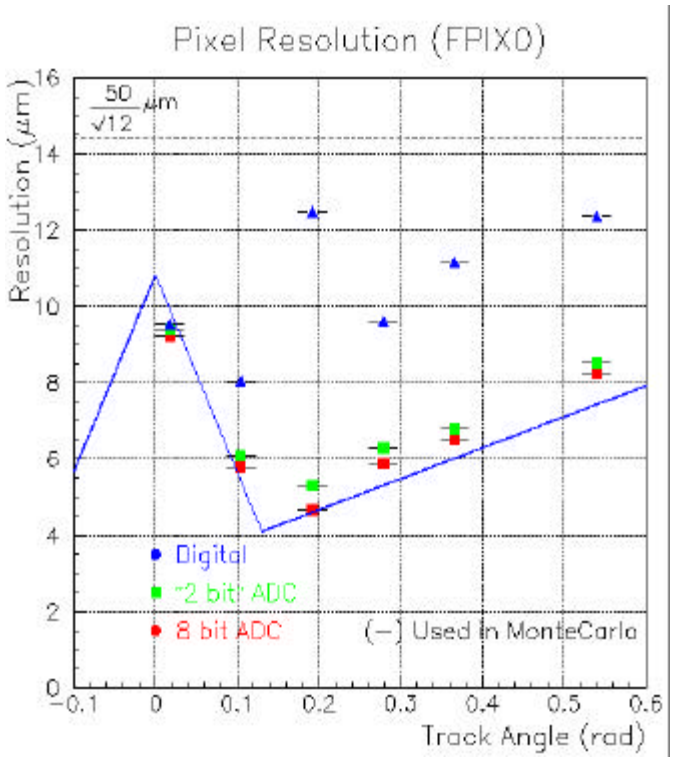




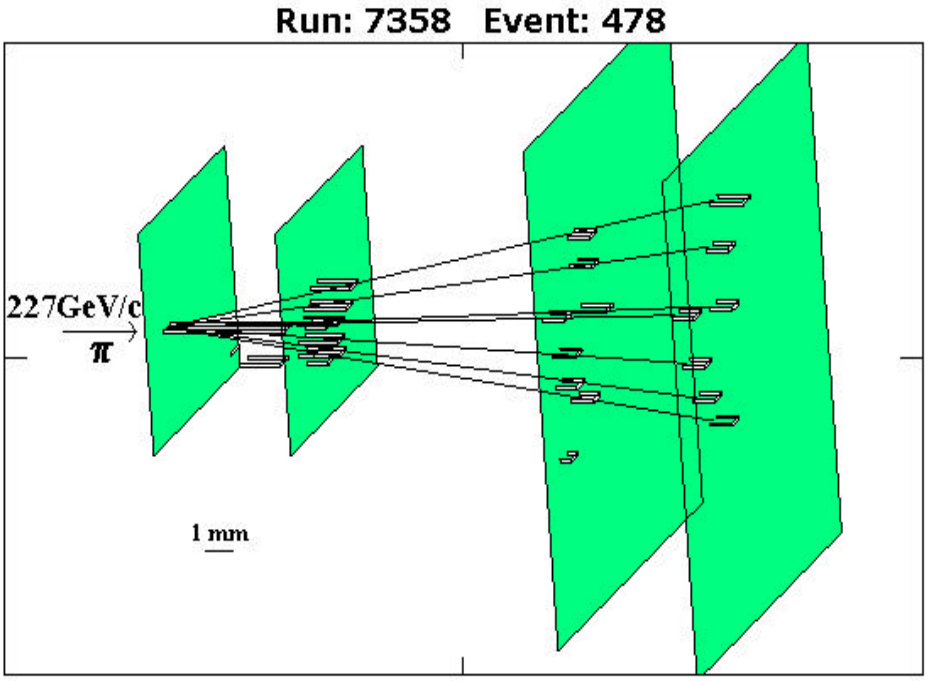


- I/O Board
  - Controls and Initializes 4 Pixel readout chips
  - GPIB controller: HV, thresholds, and pulser
- Automatic pixel calibration

Testbeam results



Position resolution better than 8 μm for most track angles



Status of pixel subgroup

- Interested groups just joining
- Fall for conceptual design
  - geometry
  - readout architecture
  - tracking performance simulation
  - integration into the inner shell
- Address questions necessary to determine whether pixels are part of the baseline plan for replacement silicon
- 2001: sensors 2002: chips
  2003: build 2004: data