

# Pixels in Run IIb

Precision tracking in the high radiation collider environment for a Higgs discovery at the Tevatron before LHC turn-on.

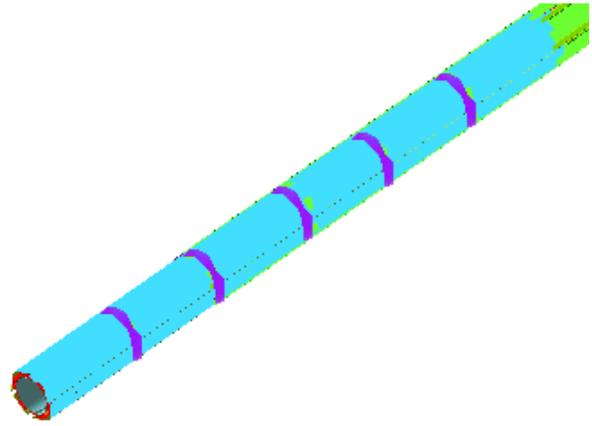
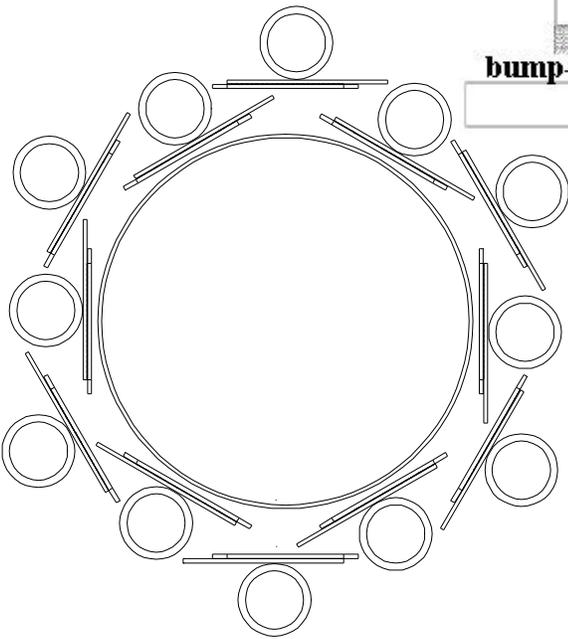
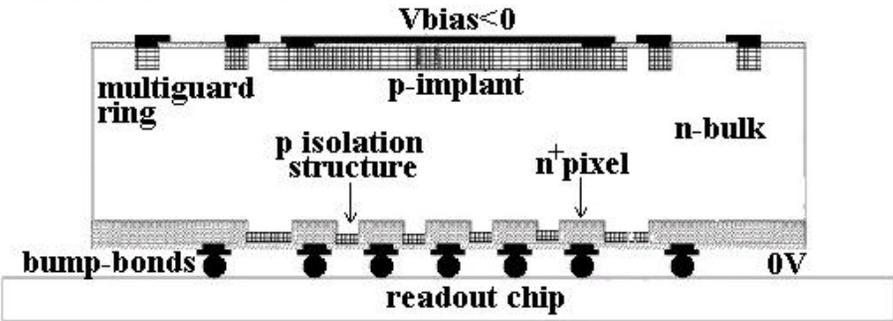
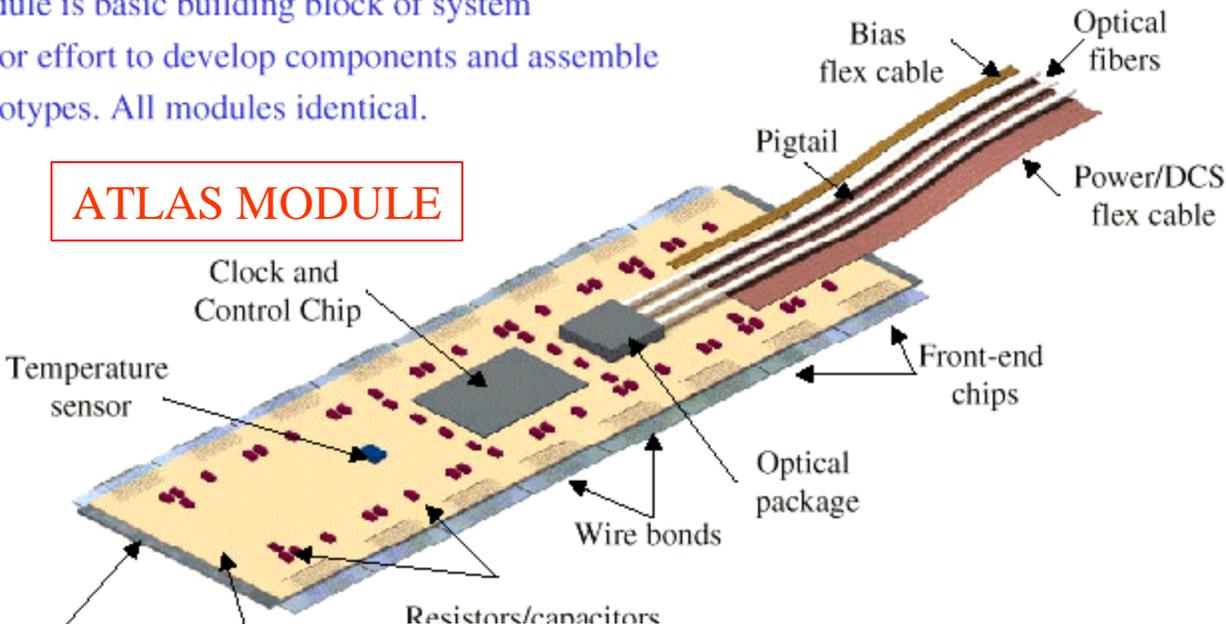
- Pixels provide advantages over other technologies at small radius
  - radiation hard to ~30 Mrad
  - large S/N (noise typically 100 e- or less)
  - pattern recognition
- Pixels are feasible using advanced R&D at FNAL and LHC
- Layer00 replacement strip option to be pursued until clear advantages and schedule non-risk are demonstrated

*Question:* Would CDFII prefer a pixel system to replace inner silicon? What questions need to be addressed to determine whether pixels become part of the baseline silicon replacement plans?

# Pixel concept

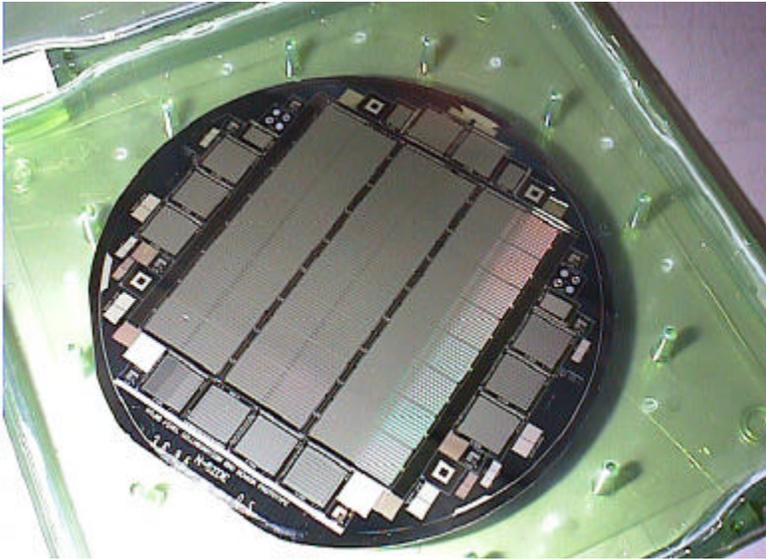
Module is basic building block of system  
 Major effort to develop components and assemble prototypes. All modules identical.

## ATLAS MODULE

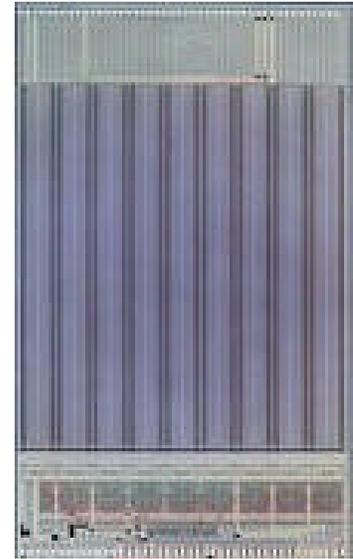


# Pixel concept

ATLAS WAFER



FPIX1 chip



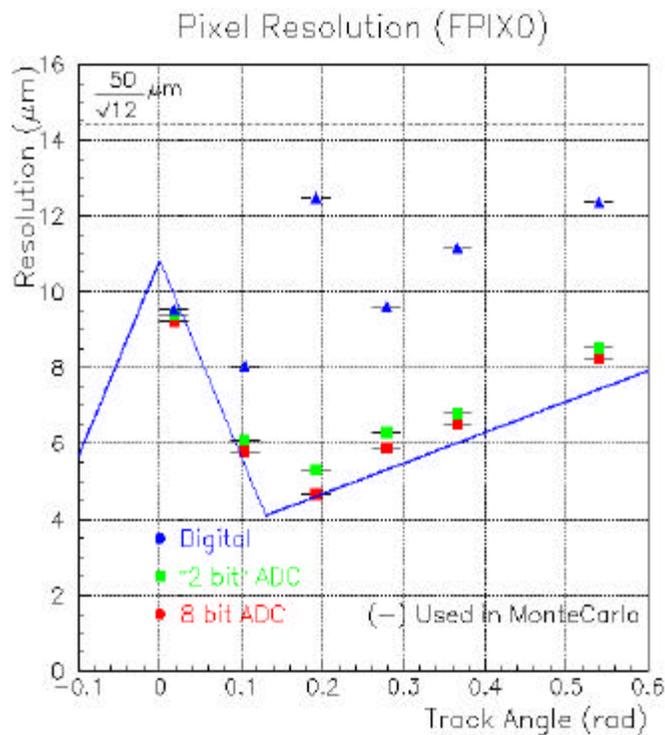
## Channel Count

Pixel cell	50 $\mu\text{m}$ x 400 $\mu\text{m}$	1 channel
Pixel cell (between readout chips)	50 $\mu\text{m}$ x 600 $\mu\text{m}$	1 channel
FPIX chip	18 columns x 160 rows	2,880 channels
Sensor/Module	single row of 8 FPIX chips	23,040 channels
Ring	12 modules in $\phi$	276,480 channels
Complete detector	12 rings along z	3, 317,760 channels

## Mechanical

FPIX chip	total area (assumes 3mm for periphery and bonding pads+100 $\mu\text{m}$ all around)	0.82 cm x 0.77 cm
FPIX chip	thickness	280 $\mu\text{m}$
Sensor	active area	0.8 cm x 5.90 cm
Sensor	total area (assumes 1mm guard ring)	1 cm x 6.10 cm
Sensor	thickness	280 $\mu\text{m}$
Sensor	inner layer innermost radius (closest surface to beam pipe)	1.33 cm
Sensor	outer layer innermost radius	1.60 cm
Detector	length in z (assumes 1.5mm between modules)	75cm

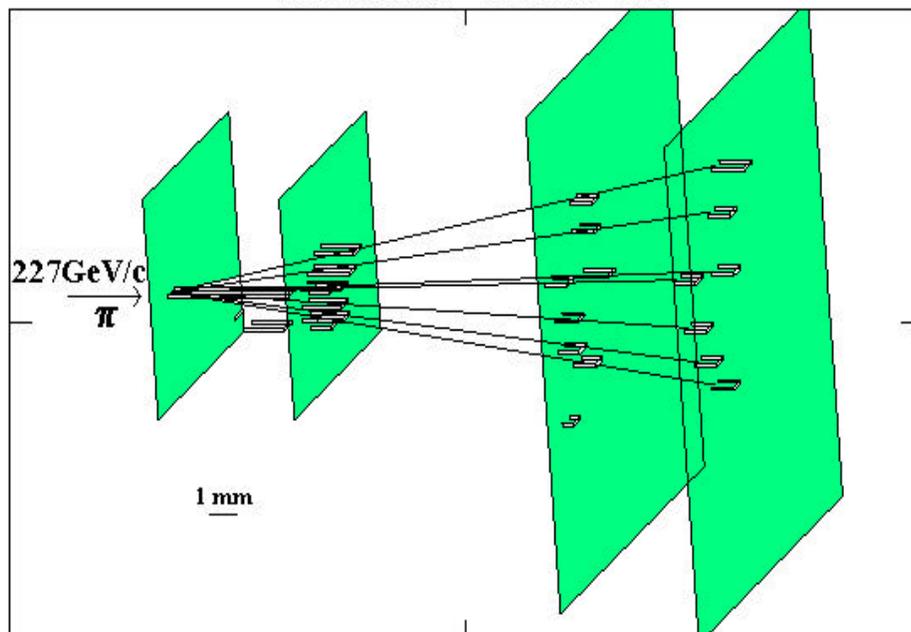
# Testbeam results



Position resolution  
better than  $8 \mu\text{m}$   
for most track angles

Large  $S/N \sim 100$  allows  
for better centroid  
finding

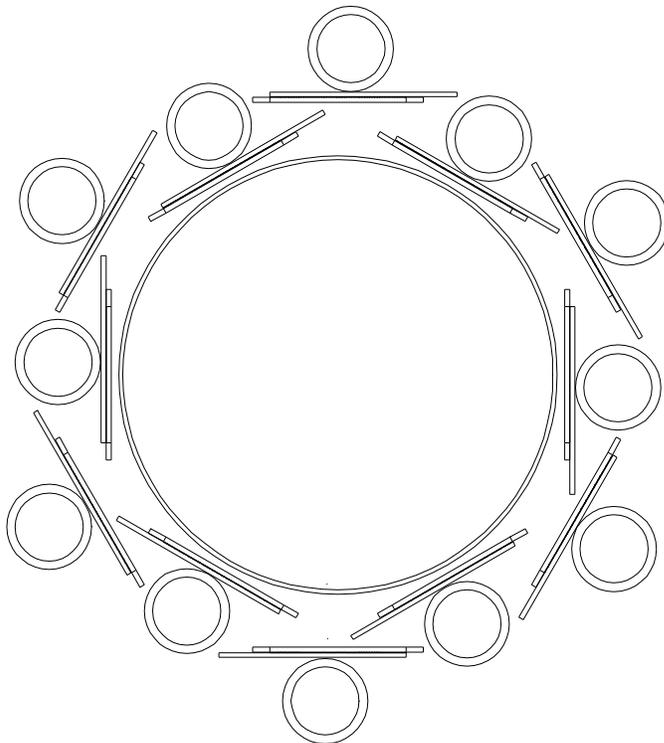
Run: 7358 Event: 478



# Material

<i>Item</i>	<i>Thickness(mm)</i>	<i>X<sub>0</sub>(mm)</i>	<i>Coverage</i>	<i>X/X<sub>0</sub>(%)</i>
<i>Sensor</i>	0.25	93.6	1.20	0.32
<i>Readout chip</i>	0.20	93.6	1.15	0.25
<i>Bumps and wire bond</i>	0.02	10.0	0.02	0.004
<i>HDI</i>	0.224	284	1.00	0.08
<i>Components on HDI</i>				0.04
<i>Glue</i>				0.02
<i>Coolant(water/alcohol)</i>	0.35	400	0.10	0.01
<i>Substrate(C - C)</i>	0.5	427	0.50	0.06
<i>Shielding(Al)</i>	0.1	89.0	1.00	0.11
<i>Total</i>				0.89

**ATLAS also has 0.7% X<sub>0</sub> for modules (no support and cooling). CMS cooling for 200W uses 12 mm<sup>2</sup> pipes.**



33% 3 Si layers

14% 4 Si layers

53% 2 Si layers+cooling

Si layer ~ 0.35% X<sub>0</sub>

cooling (2mm) ~ 2 Si layers

4 Si layer equiv=1.4% X<sub>0</sub>

Keeping material to less than 2.5% X<sub>0</sub> looks possible.

# Cost

## Overlap with BTeV 10% scale test

50 sensors @ \$2.5K = \$125K

(prototypes at \$5.5K, production \$2.5K)

10 wafers chips = \$96K

(first 10 at \$161K, next 10 at \$32K)

bump bonding ~ sensor costs

Some additional expense over strips on mechanical and cooling.

\$1M for marginal cost to the lab for a CDF pixel system is a realistic goal.

If the lab agrees to fund this project separately (helps BTeV too), does CDF want pixels?

# Status of pixel subgroup

- Interested groups just joining
- Fall for conceptual design
  - geometry
  - readout architecture
  - tracking performance simulation
  - integration into the inner shell
- Address questions necessary to determine whether pixels are part of the baseline plan for replacement silicon
- 2001: sensors    2002: chips  
2003: build        2004: data