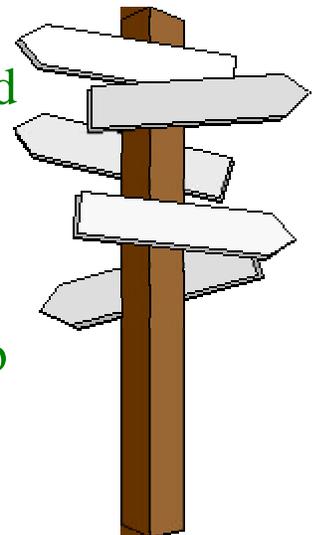


# Pixels for CDF in Run IIb

Apr 5, 2001 meeting

- Charge from directorate
  - April PAC: written document with conceptual design + resource loaded schedule/cost
  - May: PPD Review
  - June PAC: document addressing PPD/PAC comments
  - Fall: design report to be reviewed before the Fall PAC
- Meetings w/ Al, Fraco, Michael, Joe
  - Pixels likely not part of the conceptual design
    - Strips now address pattern recognition
    - Strips don't have technical challenges of material and cooling to the same degree
    - Tone should remain positive towards pixel efforts in the context of providing a possible technology that could help make the best RunIIb detector
  - Strip pattern recognition to be demonstrated
  - L00 scheme needs to be demonstrated
  - Pixels should remain a possible fall back
  - Cost of two technologies is high - need to move forward as a collaboration for RunIIb
- Michael's vision of a "physics driven, integrated tracking plan"

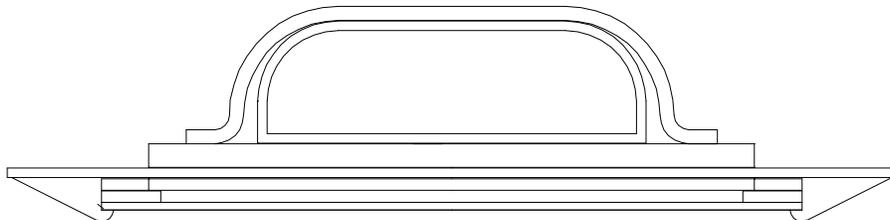


# Update

- FPIX chip
  - Nothing new on design (SVX4 has priority)
    - Pre-FPIX2-T2 works! (final prototype)
    - Core is finished
    - Periphery options are being discussed
  - April/May SEU testing at IU cyclotron
  - BTeV chip baseline has 128 rows (was 160)
- Sensors
  - Non-disclosure agreement being drafted by ATLAS pixel steering group. Next step is FNAL legal dept. ATLAS requests \$60K for this – rad hard vertex group would get prototype sensors in return
- Electronics/DAQ R&D (rad hard vtx grp)
  - Module construction (sensor, chip, HDI sandwich) is in progress
  - PCI based DAQ being commissioned – will be used for upcoming SEU tests
  - Other R&D in progress (e.g. chip thinning, UC Davis and CMU looking at readout)

# Mechanical

- 3D Modeling (Mike Hrycyk)
  - Some preference for a L00-like shell support concept over the ATLAS stave concept (8-fold geometry)
- It is excluded that a L00 pixel device could be designed to fit as a L00 only replacement
  - Fall back not excluded for a new smaller diameter beam pipe surrounded by pixels inside SVXII (disaster scenerio, no RunIIb DOE funding for a full replacement)
- Flexibility in array size keeps pixels at L00 radii or at pointing layer radii
  - Keep compatibility with either BTeV FPIX chip or ATLAS sensors
  - Double-wide sensors help HDI design.



# Material

- Estimate of 2.5%  $X_0$  still holds
  - New cooling gives more material
  - Number of HDI layers and larger active area gives less material
  - Next calculation after more mechanical design
- For pixels at L00 radius
  - Distance to i.p. more important than material
- For pixels at pointing layer
  - Single pixel layer likely to be less or similar to three low mass strip layers

# Cooling

- Power budget ~ 540W total
  - Readout chips 288 W (was 250 W)
  - Irradiated sensors 86.4 W
  - Signal cables 24W (worst case)
  - Power cables 40 – 140 W
- Greg Derylo has done some calculations (CDF 5577)
  - Ethylene glycol not adequate
    - Laminar flow / subatmospheric operation
  - C<sub>6</sub>F<sub>14</sub> in turbulent flow looks viable
    - CMS coolant choice and SiDet testing in the future
    - Also studied successfully for ATLAS
- Pixels at pointing layer could be less than 300 W
  - Binary readout gives 1/2 power to chips
  - Leakage in sensors expected to be negligible
  - Distribute power using 30AWG not on HDI

# Conclusions

- The best RunIIB detector needs better pattern recognition than the current system. Pixels at L00 or as the pointing layer achieve this.
- If single technology (strips) can do pattern recognition and improve  $z$  resolution, great!
- If not, pixels are available. A good start to a pixel group has been formed. Good visibility of pixels to the directorate / engineers exists.
- Chips + sensors can be ordered in 2001. Estimate for project at \$1.5M still holds.
- Pixels for RunIIB are achievable, how we proceed is in a large part up to this committee.